IBM No. 63-928-137

SATURN V GUIDANCE COMPUTER

(NASA-CR-155998) SATURN 5 GUIDANCE COMPUTER Semiannual Progress Report, 1 Apr. - 30 Sep. 1963 (IBM Federal Systems Div., Owego, N. Y.) 221 p

N78-74245

Unclas
00/15 56646

2000

X66 36267 X67 89751 (ACCESSION NUMBER)
221 (PAGES)
CR-74449 (NASA CR OR TMX OR AD NUMBER)
(THRU) 2A (CODE) 08 (CATEGORY)
FACILITY FORM 602

NASA Offices and Research Centers Only

FEB 1978 RECEIVED NASA STI FACILITY

IBM

Federal Systems Division
Owego, New York

NASA-13 297B

NOTICE

THIS REPRODUCTION WAS MADE FROM THE BEST AVAILABLE COPY OF WHICH A NUMBER OF PAGES WERE OF POOR REPRODUCTION QUALITY.

Saturn V Guidance Computer

Semiannual Progress Report

1 April - 30 September 1963

Contract No. NAS 8-5276

ORIGINATED BY: Saturn Computer Staff

CLASSIFICATION AND CONTENTS APPROVED BY: W. M. Dickinson

PROJECT OFFICE APPROVAL: R E Kuehn

IBM NO. 63-928-137

Prepared for the
GEORGE C. MARSHALL SPACE FLIGHT CENTER
Huntsville, Alabama

IBM Space Guidance Center, Owego, New York

~~NASA Offices and Research Centers Only~~

31 October 1963

Foreword

This semiannual progress report is submitted in accordance with the requirements of NASA Contract NAS8-5276. Included herein is a description of work performed during the period from 1 April through 30 September 1963 in fulfillment of contractual requirements.

TABLE OF CONTENTS

Section	Title	Page
I	INTRODUCTION	1-1
II	ELECTRICAL AND MECHANICAL DESIGN	2-2
	A. COMPUTER LOGIC AND CIRCUIT DESIGN	2-2
	1. COMPUTER FUNCTIONAL DESCRIPTION	2-2
	2. COMPUTER CONTROL	2-7
	3. PROGRAMMING CONSIDERATIONS	2-10
	4. ARITHMETIC ELEMENTS	2-12
	5. MEMORY	2-17
	6. COMPUTER INPUT/OUTPUT CAPABILITY	2-23
	7. LOGIC DESIGN	2-24
	8. LOGIC CIRCUITS	2-32
	9. SPECIAL CIRCUITS	2-35
	10. MEMORY CIRCUITS	2-41
	11. ULD TEST SPECIFICATIONS AND USAGE	2-47
	12. POWER SUPPLY DECOUPLING	2-47
	13. SATURN V COMPUTER FINAL RELEASE DRAWING NOMENCLATURE	2-47
	14. DELAY LINE EVALUATION	2-56
	15. MEMORY CORES, PLANES AND ARRAY EVALUATION	2-56
	B. BREADBOARD MEMORY EVALUATOR	2-61
	1. FUNCTIONAL DESCRIPTION	2-61
	2. OPERATIONAL SEQUENCE	2-63
	3. PRELIMINARY TEST RESULTS	2-65
	C. MECHANICAL DESIGN AND FABRICATION	2-65
	1. BREADBOARD COMPUTER	2-65
	2. TMR COMPUTER	2-97

Table of Contents (cont)

Section		Title	Page
II (cont)	D.	SIMPLEX COMPUTER MECHANICAL DESIGN . .	2-101
	E.	TMR COMPUTER MECHANICAL DESIGN	2-102
	1.	STRUCTURE: DIMENSIONS, VOLUME AND WEIGHT	2-102
	2.	MEMORY CONFIGURATION.	2-102
	3.	MATERIALS INVESTIGATIONS	2-114
	4.	THERMAL ANALYSIS AND TESTS	2-117
	5.	ELECTROMAGNETIC COMPATIBILITY. . .	2-120
	6.	THEORETICAL ANALYSIS.	2-120
III		LABORATORY TEST EQUIPMENT	3-1
	A.	ELECTRICAL DESIGN AND TESTING	3-2
	B.	MECHANICAL DESIGN AND FABRICATION	3-4
	1.	CABINET	3-4
	2.	OPERATOR PANELS	3-5
	3.	TAPE CONTROL SYSTEM	3-5
	4.	PRINTED-CIRCUIT CARDS	3-6
	5.	LOGIC CHASSIS GATES	3-6
	6.	DELAY LINE GATE	3-6
	7.	POWER SEQUENCING RELAY GATES	3-13
	8.	MODULE SWITCHING GATE	3-13
	9.	INTERFACE CONNECTOR PANEL ASSEMBLY	3-13
	10.	COMPUTER TEST STAND	3-13
IV		RELIABILITY	4-1
	A.	INTRODUCTION.	4-2
	B.	COMPUTER RELIABILITY ANALYSIS	4-4
	C.	SUBSYSTEM CALCULATIONS	4-5
	D.	SYSTEM ANALYSIS	4-6

Table of Contents (cont)

Section		Title	Page
IV (cont)	E.	ERROR DETECTORS	4-7
	F.	SPECIAL RELIABILITY STUDIES	4-8
		1. VOTER INTERFACE BETWEEN LOGIC AND MEMORY	4-8
		2. TIMING RELIABILITY	4-8
		3. EFFECT OF FAILURES PRIOR TO LAUNCH	4-9
		4. DISAGREEMENT DETECTOR RELIABILITY.	4-12
		5. STATISTICAL CONFIDENCE INTERVALS FOR MONTE CARLO PROGRAM RESULTS.	4-13
	G.	COMPONENT APPLICATION REVIEW.	4-14
	H.	RELIABILITY EVALUATION TESTING	4-14
		1. MIB EVALUATION TESTING	4-14
		2. COMMERCIAL MODULES	4-15
		3. INTEGRATED CIRCUITS (TEXAS INSTRUMENTS "FLAT-PACK")	4-16
		4. URD - TEMPERATURE MATRIX TEST	4-16
		5. MEMORY EVALUATION	4-18
		6. COMPONENT EVALUATION	4-18
V		QUALITY ASSURANCE	5-1
	A.	QUALITY ASSURANCE DRAWING AND SPECIFICATION REVIEW	5-2
	B.	CONTROL OF CONTRACTOR-PROCURED MATERIAL	5-2
		1. SELECTION OF PROCUREMENT SOURCES	5-2
		2. PROCUREMENT DOCUMENTATION	5-3
		3. RECEIVING INSPECTION	5-3

Table of Contents (cont)

Section		Title	Page
V (cont)	C.	CONTROL OF CONTRACTOR-BUILT ARTICLES. . .	5-5
		1. INSPECTION AND TEST PLANNING	5-5
		2. CONFORMANCE CRITERIA	5-5
		3. INSPECTION AND TEST PERFORMANCE . . .	5-5
		4. PROCESS CONTROLS	5-6
		5. QUALIFICATION OF PROCESS OPERATIONS	5-6
	D.	INSPECTION, MEASURING, AND TEST EQUIPMENT	5-7
		1. STANDARD TEST EQUIPMENT	5-7
		2. SPECIAL TEST EQUIPMENT	5-7
	E.	HANDLING AND STORAGE	5-8
	F.	TRAINING AND CERTIFICATION OF PERSONNEL .	5-8
	G.	DATA REPORTING AND CORRECTIVE ACTION . . .	5-9
		1. QUALITY DATA	5-9
		2. CORRECTIVE ACTION	5-9
	H.	INSPECTION TECHNIQUES	5-9
VI		MAINTAINABILITY	6-1
VII		FACTORY TOOLS AND TEST EQUIPMENT	7-1
	A.	GENERAL	7-2
		1. SPECIAL CIRCUITS TESTER DEVELOPMENT	7-2
		2. RESISTOR TRIMMING SIMPLIFIED PROGRAM SYSTEM	7-2
		3. PALLET.	7-3
		4. MANUFACTURING ENGINEERING	7-3

Table of Contents (cont)

Section		Title	Page
VII (cont)	B.	SIMPLEX ULD's	7-4
		1. MODIFICATION OF TWO GEMINI SEMI-AUTOMATIC CIRCUIT TEST SETS (SACTS) FOR ULD TESTING	7-4
		2. MANUAL RESISTOR TRIMMER	7-4
		3. ULD FABRICATION	7-4
		4. ULD MANUFACTURING	7-4
	C.	MEMORY	7-9
	D.	MIB's	7-9
	E.	STRUCTURE	7-10
	F.	PAGES	7-10
	G.	ULD PROTOTYPE PROGRAM	7-11
		1. GENERAL	7-11
		2. CIRCUITS/SPECIFICATIONS	7-11
Appendix		FAILURE RATE CHANGE JUSTIFICATION	A-1

LIST OF ILLUSTRATIONS

Figure	Title	Page
2-1	Computer Block Diagram	2-3
2-2	Computer Timing	2-6
2-3	MPY-DIV Timing Chart	2-10
2-4	Self-Correcting Duplex-Toroid Memory System	2-19
2-5	X-Y Coordinate Half-Select Current Error Detection	2-20
2-6	Simplex Memory Module	2-21
2-7	Typical Voter for TMR Computer	2-27
2-8	Typical Voter for Duplexed Memory Operations	2-28
2-9	Pictorial Output of the Redundancy Evaluation Program	2-33
2-10	INV Module	2-37
2-11	AA Module	2-38
2-12	Memory Clock Drivers	2-44
2-13	Breadboard Array Response Distribution	2-59
2-14	Array Response After Additional Temperature Tests	2-60
2-15	Memory Evaluator	2-62
2-16	Breadboard Computer	2-66
2-17	Page	2-67
2-18	Delay Line Page	2-68
2-19	Page Connector	2-70
2-20	Typical ULD for Simplex Breadboard Model	2-73
2-21	Flat Pack Containing Two Transistors Mounted to MIB by Solder Reflow	2-74
2-22	Cordwood Circuit Module	2-74
2-23	Leadless Semiconductor Devices Mounted to ULD Conductors	2-77
2-24	Wire-Lead Semiconductor Devices as Previously Used in Fabricating ULD's	2-77
2-25	ULD Conductor Adhesion Test	2-80
2-26	Pt-Au Tensile Bond Strength Test Fixture	2-81
2-27	Trimmed and Untrimmed Resistors on Bottom Side of ULD	2-83
2-28	Glass Strips Used to Control Solder Dimensions on Bottom Side of ULD	2-85
2-29	MIB Layers	2-87
2-30	Page MIB	2-88
2-31	Page MIB Top Land Pattern	2-89

List of Illustrations (cont)

Figure	Title	Page
2-32	Page MIB Signal Layer	2-90
2-33	Page MIB Ground Plane	2-91
2-34	Constant Stress Beam MIB	2-92
2-35	MIB Fatigue Test Installation	2-93
2-36	Breadboard Back Panel Interconnection Flat Cable	2-94
2-37	Breadboard Back Panel Interconnection Cables and Terminal Blocks	2-95
2-38	Flat Cable	2-96
2-39	Flat Cables to External Connector	2-98
2-40	TMR Computer General Layout	2-99
2-41	Back Panel Interconnection Cables	2-101
2-42	Saturn V Guidance Computer, General Design	2-103
2-43	Memory Module Design	2-104
2-44	Results of Toroid (T-38) Memory Core Test	2-110
2-45	Results of MARS (T-39) Memory Core Test (Bending and Compression)	2-111
2-46	Results of MARS (T-39) Memory Core Test (Tension)	2-112
2-47	Saturn V System Grounding Diagram	2-121
3-1	ACME Outline Drawing	3-5
3-2	Tape Control Panel	3-6
3-3	Power Control Panel	3-7
3-4	Memory Load/Data Display Panel	3-8
3-5	Interface Exerciser Panel	3-9
3-6	Tape Reader	3-10
3-7	Tape Spooler	3-10
3-8	"Translator" Printed Circuit Board Assembly	3-11
3-9	"Translator" Schematic Diagram	3-12
4-1	Computer Reliability Model	4-4
7-1	Semi-Automatic Circuit Test Set	7-5
7-2	Semi-Automatic Circuit Test Set Temperature Test Chamber	7-6
7-3	Manual Resistor Trimmer	7-7
A-1	Typical MIB Connection Configuration	A-2

LIST OF TABLES

Table	Title	Page
2-I	Data and Instruction Word Format	2-4
2-II	Operation Code Map	2-7
2-III	ULD Data - Saturn V TMR Computer With 4 Memory Modules	2-48
2-IV	Drawing Nomenclature	2-49
2-V	Simplex Computer ULD Modules	2-71
2-VI	Thermal Test Results	2-100
4-I	Saturn V Component Part Failure Rates	4-3
4-II	Computer Logic Reliability	4-5
4-III	Clock Generator and Logic Reliability	4-6
4-IV	Memory Reliability	4-6
4-V	Redundant Computer Reliability	4-7
4-VI	Nonredundant Computer Reliability	4-7
A-1	MIB Failure Rate Determination (28 ULD's/MIB)	A-3
A-2	Back Panel Failure Rate Determination	A-4
A-3	Hardware Listing	A-5
A-4	Reapportionment Table	A-6
A-5	Adjusted Failure Rates and Conditional Probability of Open	A-6
A-6	Single Channel Timing Generator Failure Rates	A-7
A-7	Single Channel TMR Logic Substrate Failure Rate	A-7
A-8	Single Channel Logic Component Count	A-8

Section I

Introduction

Section I

Introduction

Significant progress has been made during this reporting period in the design of the Saturn V breadboard computer. The logic for the triple modular redundant (TMR) version was released and then abstracted to derive the logic for the simplex computer. With this release, the computer design was subdivided into pages. The artwork for the multilayer interconnection boards (MIB's) on each page has been released to manufacturing along with the artwork for the unitized logic device (ULD) circuits involved in the design. The design for the back panels that are used to interconnect the pages has also been released. The computer structure is being built from sheet metal.

A breadboard memory was built using toroid cores and commercial memory-plane frames that were reworked to the Saturn V configuration. The memory electronics was assembled on standard modular system (SMS) cards, and the entire unit is undergoing laboratory evaluation.

A liquid-cooled prototype structure for the TMR computer is being developed and several methods for building the structure are being evaluated. Magnesium-lithium billets, which will be machined for the experimental structural units, have been ordered.

The design progress for the aerospace computer manual excerciser (ACME) has paralleled that of the basic hardware; the electrical and mechanical design has been completed, the necessary parts have been ordered, and assembly of the first ACME has begun. It will be ready for use in the build-up and check-out of the breadboard computer.

Reliability studies of the computer design were performed using the IBM 7090 reliability simulation program in conjunction with manual and IBM 1620 computations. Based on the present configuration of a TMR central computer and duplexed memories, the results of the reliability studies indicate that the TMR computer will more than meet its reliability goals. In addition to the previously mentioned studies, numerous other special reliability evaluations were conducted.

Component testing has been carried out and planning performed for future larger-scale tests of components and subassemblies to be used in prototype computers. The results of step-stress tests conducted at the IBM Components Division have been studied.

Quality control personnel set up quality control practices on the ULD line and planned activities for the quality assurance program to be applied to the prototype hardware. In addition,the following were also carried out: (1) documentation of quality procedures, (2) review of routings and process control procedures, (3) qualification of special test equipment, (4) monitoring of defective parts, and (5) studies of training and certification of personnel.

Maintainability studies were conducted that included: (1) discussions with NASA personnel on laboratory test equipment (LTE) requirements and over-all check-out philosophy, (2) the design study of the computer handling fixtures and page test-point adapter, (3) establishing a maintainability requirements specification setting maintainability design requirements, and (4) the review of computer and LTE designs.

A ULD fabrication line was established to permit manufacture of the breadboard computer. This line is currently processing numerous orders for ULD's for the breadboard computer. An integrated photographic tool generation (artwork) facility (IBM-funded capital equipment) for MIB's has also been set up for the cutting of master artwork and preparation of masters for the production line. Special test equipment (some of which is IBM-funded capital equipment) required for the ULD line and for memory construction has also been designed and built.

Details of these accomplishments are contained in the following sections of this technical summary report. In many cases the results are summarized rather than presented in detail. Reports and test results substantiate the information presented.

Section II

Electrical and Mechanical Design

Section II

Electrical and Mechanical Design

A. COMPUTER LOGIC AND CIRCUIT DESIGN

1. COMPUTER FUNCTIONAL DESCRIPTION

Figure 2-1 illustrates the computer information flow. This simplified block diagram depicts the major data flow paths and associated register level logic.

The computer has been organized as a serial, fixed point, stored program, general purpose machine which processes data using "two's complement" arithmetic. Two's complement arithmetic obviates the recomplementation cycle needed when using "sign-plus-magnitude" arithmetic. Special algorithms have been developed and implemented for multiplication and division of two's complement numbers. Multiplication is done four bits at a time and division two bits at a time. These algorithms are treated separately in the Arithmetic portion of this section.

A random-access magnetic core memory will be used as the computer storage unit. A serial data rate of 512 kilobits-per-second will be maintained by operating the memory units in a serial-by-byte, parallel-by-bit operating mode. This allows the memory to work with a serial arithmetic unit. The parallel read-write word length of 14 bits includes one parity bit to allow checking of the memory operations.

Storage external to the memory is located predominantly in the shift register area. The reliability in this area is maximized by using glass delay lines for arithmetic registers and counters. Delay lines are the best choice when transistor count for the various registers is considered.

a. Organization

Each instruction comprises a four-bit operation code and a nine-bit operand address. The nine-bit address allows 512 locations to be directly addressed. The total memory is divided into sectors of 256 words, and contains a residual memory of 256 words. The nine-bit address specifies a location in either the previously selected sector (Data Sector Latches) or in the residual memory. If the operand address bit, A9, is a binary "0", then the

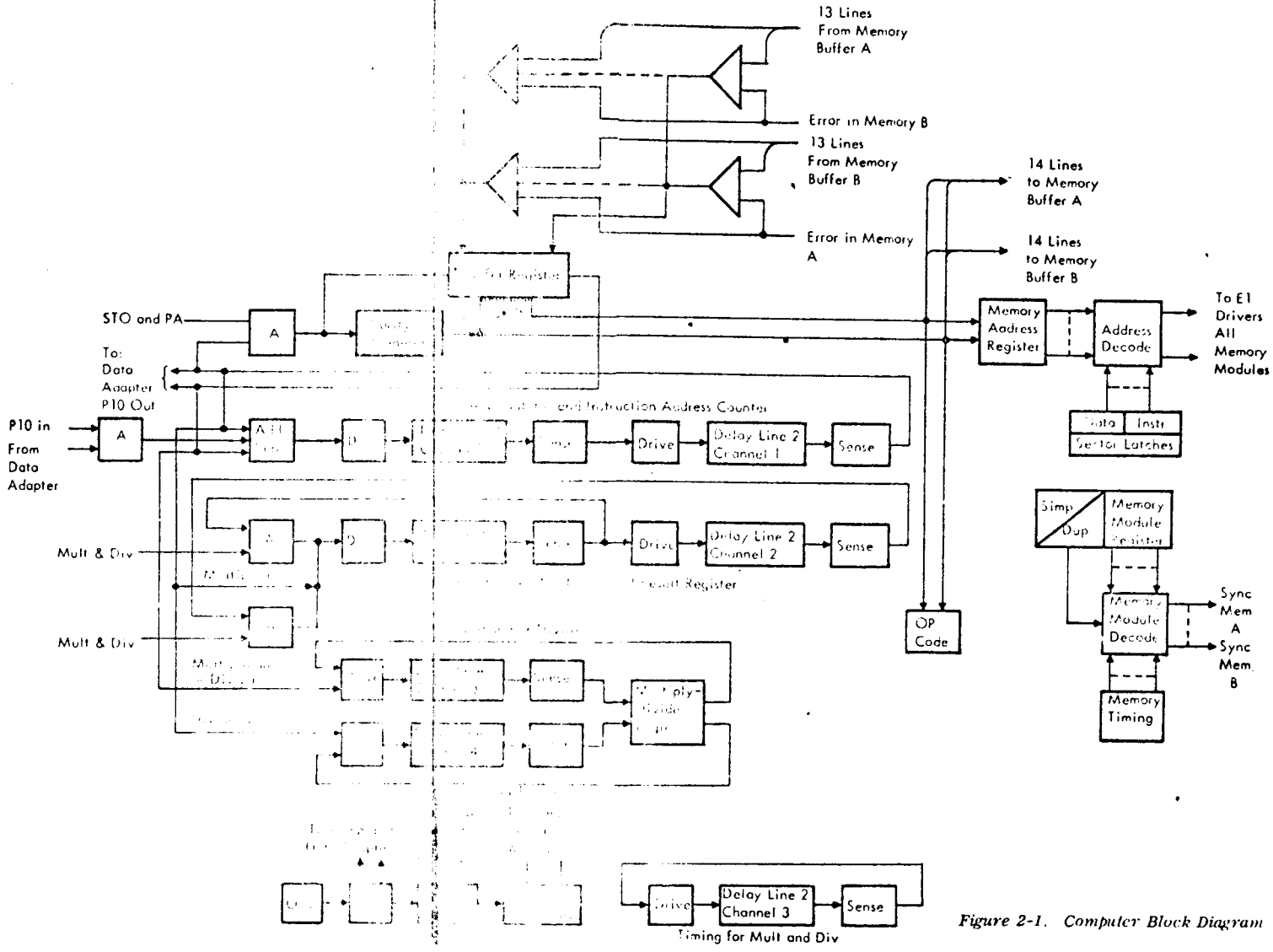


Figure 2-1. Computer Block Diagram

data will come from the sector specified by the sector register. If A9 is a "1", the second register is disregarded and the data comes from residual memory. Instructions are addressed from an eight-bit instruction counter which is augmented by a four-bit instruction sector register. Sector memory selection is changed by special instructions which change the contents of the sector register. The sector size is large enough so that this is not a frequent operation.

Data words consist of 26 bits. Instruction words consist of 13 bits and are packed in memory, two instructions per data word. Hence, instructions are described as being stored in syllable one or syllable two of a memory word. Two additional bits are used in the memory to provide parity checking for each of the two syllables. (See Table 2-I.)

The computer is programmed by means of single-address instructions. Each instruction specifies an operation and an operand address. Instructions are addressed sequentially from memory under control of the instruction counter; and each time the instruction counter is used, it is incremented by one to develop the address of the next instruction. After the instruction is read from memory and parity checked, the operation code is sent from the transfer register to the OP code register. This is a static register which stores the operation over the duration of the execution cycle.

Table 2-I

Data and Instruction Word Format

Memory Plane	Syllable 2	1	2----------					13	14
	Syllable 1	15	16----------					27	28
Data Word	Syllable 2	S	2^{-1}----------					2^{-12}	P
	Syllable 1	2^{-13}	2^{-14}----------					2^{-25}	P
Instruction Word	Syllable 1 or 1 or 2	A9	A8---A1	OP4	OP3	OP2	OP1	P	

S . . . . . Sign Position
A9, A8, A7, etc., ... Operand Address
OP1, OP2, etc., ... Operation Codes
P . . . . . Parity Bit

The operand address portion of the instruction is transferred in parallel (9 bits) from the computer's transfer register (TR) to the memory address register. The TR is then cleared. If the operation code is one which requires reading the memory, the contents of the operand address are read 14 bits at a time (including parity) from the memory into the buffer register where a parity check is made. Data bits are then sent in parallel to the TR. This information is then serially transferred to the arithmetic section of the computer. If the operation code is a store (STO) the contents of the accumulator are transferred serially into the TR and stored in two 14-bit bytes. A parity bit is generated for each byte.

Upon completion of the arithmetic operation, the contents of the instruction counter are transferred serially into the TR. This information is then transferred in parallel (just as the operand address had previously been transferred) into the memory address register. The TR is then cleared and the next instruction is read, thus completing one computer cycle.

The data word is read from the memory address specified by the memory address register and from the sector specified by the sector register. Data from the memory goes directly to the arithmetic section of the computer where it is operated on as directed by the OP code. The arithmetic section contains an add-subtract element, a multiply-divide element, and a storage register for the operands. Registers are required for the accumulator, product, quotient, multiplicand, multiplier, remainder, and divisor. The add-subtract and the multiply-divide elements operate independently of each other. Therefore, they can be programmed to operate concurrently if desired; i.e., the add-subtract element can do several short operations while the multiply-divide element is in operation. No dividend register is shown in Figure 2-1 because it is considered to be the first remainder. As indicated, both multiply and divide require more time for execution than the rest of the computer operations. A special counter is implemented to keep track of the multiple-divide progress and stop the operation when it is completed. The product-quotient (PQ) register has been assigned an address and is addressable from the operand address of any instruction. The answer will remain in the PQ register until multiply-divide is initiated.

b. Timing

The three levels of computer timing are illustrated in Figure 2-2. Basically, the computer is organized around a four-clock system. The width of each clock is approximately 0.4 usec and the pulse repetition frequency is 512 kilocycles. The bit time (four clock pulses) is 1/.512 usec. Fourteen bit times occur in one phase time, resulting in a phase time of 27.34375 usec. Three phase times (P_A, P_B, and P_C) are required to perform a complete computer operation cycle. Phase A (P_A) makes up the instruction cycle, and phases B and C (P_B and P_C) determine the data cycle.

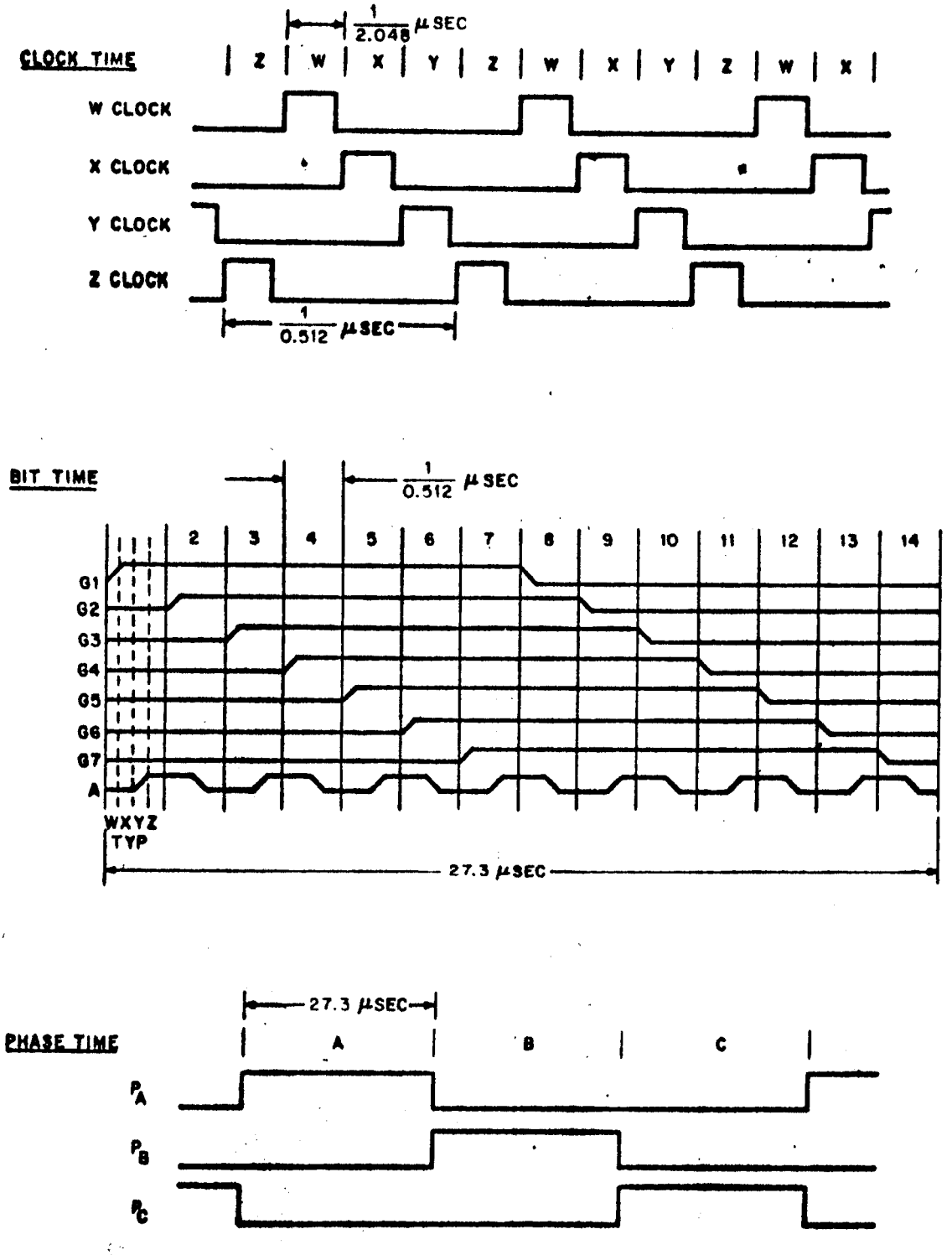


Figure 2-2. Computer Timing

2. COMPUTER CONTROL

a. Instruction List

The instruction bit assignment for the operation code is shown in Table 2-II.

Table 2-II

Operation Code Map

OP2

OP1				
	MPY		STO	DIV
	MPH	XOR	CLA	ADD
	TNZ	TMI	SHF	AND
	HOP	TRA	PIO	SUB

OP3

OP4

HOP (82 usec) 0000 — The contents of the memory address designated by the operand address specify the next instruction address and data sector. Four bits identify the next instruction sector, eight bits are transferred to the instruction address counter, one bit conditions the syllable control, four bits identify the next data sector, three bits identify the next memory module, one bit defines either a simplex or duplex memory operation, and one bit resets the memory error latch when specifying a new memory module.

TRA (82 usec) 1000 — The eight-bit operand address is transferred to the instruction counter. The residual bit in the operand address is used to specify the instruction syllable latch. The sector register remains unchanged.

TMI (82 usec) 1100 — A transfer occurs on the minus accumulator sign. If the sign is positive, the next instruction in sequence is chosen (no branch); if the sign is negative (zero is considered positive), the eight-bit operand address becomes the next instruction address (perform branch), and a TRA operation is executed.

TNZ (82 usec) 0100	A transfer occurs when the accumulator contains a non-zero number. If the accumulator is zero, the next instruction in sequence is chosen; if the accumulator is not zero (either negative or positive), the eight-bit operand address becomes the next instruction address, and a TRA operation is executed.
SHF (82 usec) 1110	The SHF instruction shifts the accumulator contents right or left one or two places as specified by the operand address. A1 Right Shift 1 A5 Left Shift 1 A2 Right Shift 2 A6 Left Shift 2
AND (82 usec) 0110	The contents of the memory location specified by the operand address are logically AND'ed, bit-by-bit, with the accumulator contents. The result is retained in the accumulator.
CLA (82 usec) 1111	The contents of the location specified by the operand address are transferred to the accumulator.
ADD (82 usec) 0111	The contents of the location specified by the operand address are added to the accumulator contents. The result is retained in the accumulator.
SUB (82 usec) 0010	The contents of the location specified by the operand address are subtracted from the accumulator contents. The result is retained in the accumulator.
STO (82 usec) 1011	The contents of the accumulator are stored in the location specified by the operand address as well as being retained in the accumulator.
DIV (656 usec) 0011	The contents of the accumulator are divided by the contents of the memory location specified by the operand address. The 24-bit quotient is contained in the product-quotient delay line. Concurrent use of the adder-subtractor element is permitted.
MPY (328 usec) 0001	The contents of the memory location specified by the operand address are multiplied by the accumulator contents. The 24 high-order bits of the multiplier and multiplicand are multiplied together to form a 24-bit product. Concurrent use of the add-subtract element is permitted. The product is stored in the product-quotient delay line.

MPH (410 usec) 0101	This is the multiply and hold operation. It is the same as the MPY operation except concurrent use of the add-subtract element is not permitted and the product is stored in the accumulator.
XOR (82 usec) 1101	The contents of the memory location specified by the operand address are exclusively OR'd, bit-by-bit, with the contents of the accumulator. The result is retained in the accumulator.
PIO (82 usec) 1010	The low-order address bits, A1 and A2, determine whether the operation is an input or output instruction. The high-order address bits, A8 and A9, determine whether the data contents are transferred from the main memory, residual memory, or accumulator.

b. Multiply and Divide Timing

All operations, except MPY, MPH, and DIV require one operational cycle (82 usec) for execution. Other instructions must be executed concurrently with the MPY and DIV instructions (except MPH). Three instructions can be executed between the initiation of the MPY and the time when the product is available; similarly, seven instructions can be executed between the initiation and the termination of DIV. More one-word-time instructions can be inserted before the product or quotient is addressed if maximum efficiency is not required, since multiplication or division is stopped automatically and the result retained until addressed. Figure 2-3 illustrates the timing of the MPY and DIV operations. The MPH instruction cannot operate concurrently with other operations because it inhibits further memory accesses until completed.

c. Interrupt

A program interrupt feature is provided to aid the input/output processing. An external signal interrupts the computer program and causes a transfer to a subprogram. Interrupt occurs when the instruction in progress is completed. The instruction counter, sector and module registers, and syllable latch are stored automatically in a reserved residual memory location (octal address 777). A HOP constant which designates the start of the subprogram is subsequently retrieved from a second reserved residual memory location (octal address 776). Automatic storage of the accumulator and product-quotient registers is not provided; this must be accomplished by the subprogram. Multiple interrupt protection or interrupts during MPY and DIV operations are provided.

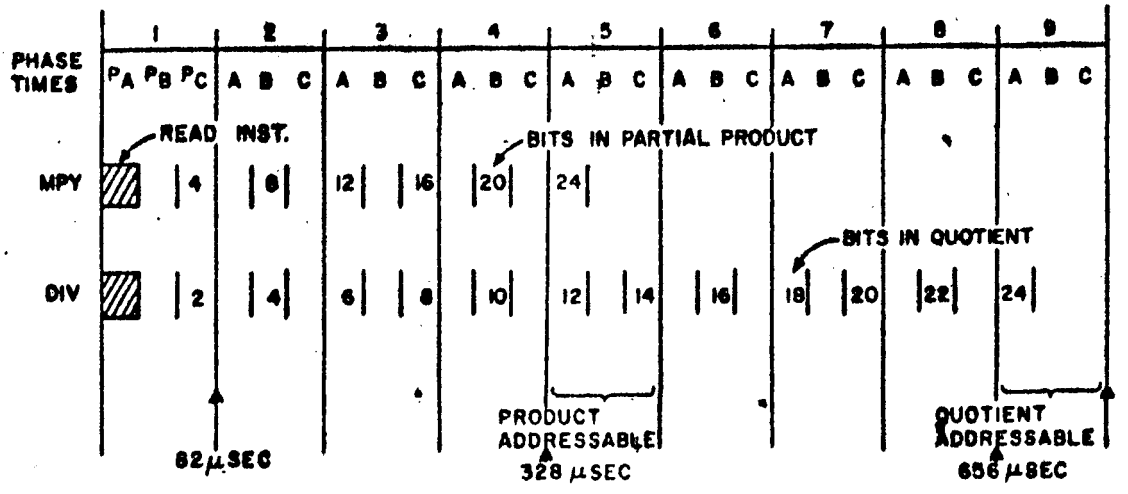


Figure 2-3. MPY-DIV Timing Chart

The interrupt signal may be generated by a timed source. The rate at which it is generated will be program controlled by changing the magnitude of a number, which is being continually summed. When the summed number reaches a predetermined value, the interrupt signal is generated. The main program can be resumed by addressing the contents of residual memory word 777 with a HOP instruction.

Other external signals such as discrete inputs will also be allowed to cause interrupt. These signals will be useful in causing the I/O subprogram to give immediate attention to an input or output event.

3. PROGRAMMING CONSIDERATIONS

The Saturn V Guidance Computer uses a conventional repertoire of arithmetic instructions including add, subtract, multiply, and divide; two multiply instructions are included. MPY requires one-word-time operations in the adder unit during the multiplication process because the instruction counter advances once each word time. This procedure is useful in speeding up the computer operation by permitting simultaneous multiplication and one-word operations. Trial programming has shown a speed increase for a similar configuration of up to 40 percent over a conventional

sequential organization. When the program is multiply-limited and a sufficient number of useful one-word operations cannot be located in the portion of the flow diagram being executed, the MPH instruction is used. This instruction inhibits the advance of the instruction counter so no new instructions are read from memory until the MPH operation is completed. This feature conserves program steps relative to an organization which does not contain a MPH-type operation code. Both types of multiply orders permit the increased speed of a concurrent operation without sacrifice in the number of program steps required, and permit a programming trade-off of speed and instructions required.

TRA, TMI, and TNZ instructions provide flexibility in programming unconditional transfers; in branch instructions, through transfer on the contents of the accumulator; and in easy handling of discrete inputs, which are obtained in the accumulator through masking with an AND instruction.

The HOP instruction is used for transfers outside of the sector currently being used. HOP permits jumping to another portion of the flow diagram and to subroutines. To return from a subroutine, the last instruction in the routine is a HOP. The HOP constant causes a return to the original program sequence. Since each use of a subroutine in the program results in return to a different place in the flow diagram, the HOP constant is loaded prior to entering the routine. An automatic program compiler could be used to generate the correct HOP constants.

An exclusive OR operation, XOR, permits the rapid checking of changes in discrete inputs which are grouped into data word inputs. Discrete output words may be generated by masking out the bit to be changed with an AND instruction and by adding the discrete output into the selected position. The product-quotient (P-Q) register can be addressed (by octal 775) with the operations CLA, ADD, SUB, STO, AND and XOR.

An interrupt feature is provided in the guidance computer to facilitate the timing of I/O operations by causing a transfer to an I/O subprogram. The interrupt signal may be set to interrupt at the highest rate at which any I/O quantity must be handled. The timed interrupt thereby avoids the necessity of keeping track of the time expired since last entering the I/O subprogram. Otherwise many instructions would be required in the various branches of variable length in the flow diagram. An automatic interrupt is also provided to permit certain discrete inputs to cause interrupts. While all applications for this feature have not yet been defined, allowing discretes to interrupt can be used to demand that the program give attention to an important discrete. Communications between the guidance computer and the vehicle telemetry monitoring system can thus be facilitated. The monitor system may be selected by an address code from the computer, and the

vehicle parameter to be monitored can be defined over the output line to the data adapter and stored in a buffer register. When the monitor has acquired the desired parameter, an interrupt can be given, causing the computer I/O subprogram to read the value as an input. This scheme will permit computing to continue while waiting for the monitor system to acquire the parameter.

The sector register permits considerable flexibility in handling data and constants. The instructions indicate whether data is located in the residual sector or the sector referred to by the data sector register. By confining data to the residual register and a limited number of other memory sectors, the changing of the data sector register can be minimized. In this manner, the residual sector is reduced in size and made more readily usable for data, which are referred to by instructions stored in many sectors. The small size of each sector, achieved by concentrating instructions rather than both data and instructions in each sector, reduces the size of the instruction word and conserves memory core planes. The programmer is free to move between disjointed parts of the program without frequently changing either instruction or data sector registers. The data sector register is also useful in addressing sets of constants, which are stored for use with polynomial injection guidance equations. The instructions necessary to compute the polynominals are stored once while the sets of coefficients for the many different polynomials are each stored in different memory sectors. These coefficients can be readily accessed by use of the data address register, which is set to select a given set of coefficients to evaluate the polynomial. Thus, the polynomial number is set in the sector register and the coefficients are selected.

The separate instructions and the data sector register feature eliminate the need for indexing, since it accomplishes the same end in polynomial evaluation (the chief application of indexing). Hardware and instruction bits are both saved by omitting indexing.

IBM plans to store upper and lower limits for orbital check-out parameters in the two halves of a data word. The monitoring system will relate the address of the parameter to the storage location in memory. A simple, regular sequence of addresses will make programming easy by use of address modification techniques.

4. ARITHMETIC ELEMENTS

The Saturn V Guidance Computer has two independent arithmetic elements the add-subtract element and the multiply-divide element. Although both operate independently, they are serviced by the same program control circuits and may be operated concurrently. Each program cycle time, the add-subtract element can perform any one of the computer instructions,

except MPY, MPH, and DIV. During each program cycle time, the results of the simple arithmetic operations are circulated through the accumulator delay line and through the accumulator sync delay line channel to prevent their precessing.

The multiply-divide element uses two channels of a delay line as previously shown in Figure 2-1. One channel of the instruction counter delay line is used as a counter to stop the multiply or divide operations. Another channel of the instruction counter delay line is used to sync the product or quotient when the operation is completed. This is controlled automatically by the counter. The product-quotient register is addressable as a residual memory word and has the octal address of 775. The product or quotient can be obtained on any subsequent operation cycle after completion of the multiply or divide, but must be used before initiation of another multiply or divide. The product of the MPH operation is stored in the accumulator.

The recursion formulas for implementing multiply and divide with two's complement numbers are explained in the following paragraphs.

a. Multiply

The multiply element operates in a two-phase cycle, serial-by-four parallel, and requires 15 phase times, including instruction access time. The program initiates a multiply by placing the 24 high-order bits, contained in the memory location specified by the operand address, in the multiplicand delay line. The multiplier delay line contains the 24 high-order bits of the contents of the accumulator. The phase counter terminates a multiply at the proper time following the original MPY or MPH instruction.

The instrumentation of the multiply algorithm requires three delay line channels. Two of the channels contain the partial product and the multiplier. These channels shift both the partial product and the multiplier four places to the right every two-phase cycle. The third channel contains the multiplicand. The accumulator portion (fourth channel) of this delay line is not involved in the multiply element and can be used concurrently with multiply.

Upon initiation of a multiply, and during every phase time thereafter, the five low-order bits of the multiplier (MR_1 through MR_5) are used to condition latches or tratches. These latches or tratches in turn initiate addition or subtraction of multiples of the multiplicand, to the partial product.

The following algorithm is used for multiply:

$$P_i = 1/16 \left[P_{(i-1)} + \Delta 1 + \Delta 2\right]$$

where P_i is the new partial product, and $\Delta 1$ and $\Delta 2$ are formed according to the following rules:

MR_1	MR_2	MR_3	$\Delta 1$	
MR_3	MR_4	MR_5		$\Delta 2$
0	0	0	0	0
1	0	0	+2M	+8M
0	1	0	+2M	+8M
1	1	0	+4M	+16M
0	0	1	-4M	-16M
1	0	1	-2M	-8M
0	1	1	-2M	-8M
1	1	1	0	0

M represents the multiplicand. For the first multiplication cycle, $P_{(i-1)}$ and MR_1 are made zeros.

b. Divide

The divide element operates in a two-phase cycle, serial-by-two-parallel, and requires 27 phase times per divide, including instruction access time. The program initiates a divide by transferring the 26 bits of the addressed memory location (divisor) and the 26 bits of the accumulator (dividend) to the divide element. The phase counter terminates a divide at the proper time following the original divide instruction.

The following algorithm is instrumented as follows to execute divide:

$$Q_i = R_{is} \cdot DV_S + \overline{R_{is}} \cdot \overline{DV_S} \quad (1)$$

and

$$R_{i+1} = 2R_i + (1 - 2Q_i)\, DV \quad (2)$$

where

i = 1, 2, 3, ...24

Q_i = The i^{th} quotient bit

R_{is} = The sign of the i^{th} remainder

DV_S = The sign of the divisor

R_i = The i^{th} remainder

R_1 = The dividend

DV = The divisor

Equation (1) states that the i^{th} quotient bit is equal to a "1" if the sign of the i^{th} remainder is identical to the sign of the divisor. The high-order quotient bit (sign bit) is the only exception to this rule. Q_1, as determined by Equation (1), is used to solve Equation (2) but must be complemented before it is stored as the sign of the quotient.

The instrumentation of the divide algorithm requires three channels of a delay line. One channel contains the quotient, one the divisor, and one the dividend. These three channels are used during multiply to contain the multiplier, the multiplicand, and the partial product, respectively. The quotient and the remainder channels of the delay line have been lengthened by latches to shift two places to the left each two-phase cycle. The divisor circulates once each two-phase cycle.

In the two's-complement number system, the high-order bit determines the sign of the number. Since this is the last bit read from memory, it is impossible to solve Equations (1) or (2) until the entire divisor has been read from memory. However, Equations (1) and (2) can have only two possible solutions:

Either

$$Q_i = 1$$

and,

$$R_{(i+1)} = 2\,R_i - DV$$

or,

$$Q_i = 0$$

and,

$$R_{(i+1)} = 2\,R_i + DV$$

Both the borrow of $2R_i$ - DV and the carry of $2R_i$ + DV are generated as the dividend and divisor registers are loaded. When the sign bits of these quantities are finally entered into their respective registers, Equation (1) is solved for the first quotient bit. If this quotient bit is a "1", the borrow is examined to determine the second quotient bit. If the first quotient bit is a "0", the carry is examined to determine the second quotient bit. The following truth table is solved to determine the second quotient bit. If the first quotient bit is a "1":

R_1	DV_S	B	$R_{(i+1)_S}$	Q
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Where,

R_1 = The first remainder bit to the right of the sign bit

DV_S = The divisor sign

B = The borrow into the R_1, DV_S, position

$R_{(i+1)_S}$ = The sign of the new remainder

Q = The quotient bit as determined by comparing DV_S with $R_{(i+1)_S}$ according to Equation (2).

$$Q = \overline{R}_1 \, \overline{DV}_S \cdot \overline{B} + \overline{R}_1 \, DV_S \, \overline{B} + R_1 \cdot \overline{DV}_S \cdot B + R_1 \cdot DV_S \cdot B$$

$$= \overline{R}_1 \cdot \overline{B} \, (\overline{DV}_S + DV_S) + R_1 \cdot B \, (\overline{DV}_S + DV_S)$$

$$= \overline{R}_1 \cdot \overline{B} + R_1 \cdot B$$

The equation used in generating the new remainder, R_{i+2}, is obtained by expanding Equation (2).

$$R_{(i+2)} = 2 \, R_{(i+1)} + (1 - 2 \, Q_{(i+1)}) \, DV$$

$$R_{(i+2)} = 2 \left[2R_i + (1 - 2 \, Q_i) \, DV \right] + (1 - 2 \, Q_{(i+1)}) \, DV$$

$$R_{(i+2)} = 4 \, R_i + 2 \, (1 - 2 \, Q_i) \, DV + (1 - 2Q_{(i+1)}) \, DV$$

As $R_{(i+2)}$ is being generated the next iteration of divide is started by generating, as already described, the borrow and carry for 2 $R_{(i+2)} \pm DV$.

5. MEMORY

The memory for the Saturn V Guidance Computer uses conventional toroidal cores in a unique self-correcting duplex system. The memory unit consists of six identical 4000-word memory modules which may be operated in simplex for increased storage capability or in duplex pairs for high reliability. The basic computer program can be loaded into the instruction and constants sectors of the memory, at electronic speeds, on the ground or just prior to launch. Thereafter, the information content of constants and data can be electrically altered but only under control of the computer program.

The self-correcting duplex system uses an odd parity bit with detection schemes for malfunction indication and correction. In conjunction with this scheme, error-detection circuitry is also used for memory drive current monitoring. Unlike conventional toroid random-access memories, the self-correcting extension of the basic duplex approach permits regeneration of correct information after transients or intermittent failures. Otherwise destructive read-out of the memory could result.

a. Basic Memory System Operation

Figure 2-4 shows a simplified block diagram of the computer memory system. The basic configuration consists of a pair of memories providing storage for 8192 14-bit memory words for duplex operation, or 16,384 14-bit memory words for simplex operation. Each of the simplex memories includes independent peripheral instrumentation consisting of timing, control, address drivers, inhibit drivers, sense amplifiers, error detection circuitry and I/O connections to facilitate failure isolation. Computer functions which are common to these simplex units consist of the following:

- Memory address register outputs
- Memory transfer register input-output
- Store gate command
- Read gate command
- Syllable control gates

The computer functions, which are separate for each simplex memory, consist of synchronizing gates which provide the serial data rate of 512 kilobits per second. This data rate is required by the computer to generate a start memory unit command at 128 kilobits per second. These gates also provide the selection of multiple simplex memory units for storage flexibility and permit partial or total duplex operation throughout the mission profile to extend the mean-time-before-failure for long mission times. Each of the simplex units can operate independently of the others or in a duplex manner. The memory modules are divided into two groups: one group consisting of even numbered modules (0-6); and the other consisting of odd numbered modules (1-7). There is a buffer register associated with each group which is set by the selected modules.

For duplex operation, as shown in Figure 2-4, each memory is under control of independent buffer registers when both memories are operating without failure. Both memories are simultaneously read and updated, 14 bits in parallel. A single cycle is required for reading instructions (13 bits plus 1 parity bit per instruction word). Two memory cycles are required for reading and updating data (26 bits plus 2 parity bits). The parallel outputs of the memory buffer registers are serialized at a 512-kilobit rate by the memory transfer register under control of the memory select logic. Initially, only one buffer register output is used but both buffer register outputs are simultaneously parity checked in parallel. When an error is detected in the memory being used, operation immediately transfers to the other memory. Both memories are then regenerated by the buffer register of the "good" memory, thus correcting transient errors. After the parity-checking and error-detection circuits have verified that the erroneous memory has been corrected, operation returns to the condition where each memory is under control of its own buffer register. Operation is not transferred to the previously erroneous memory until the "good" memory develops its first error. Consequently, instantaneous switching from one memory output to another permits uninterrupted computer operation until simultaneous failures at the same location in both memories cause complete system failure.

Proper operation of the memory system during read cycles is indicated by each 14-bit word containing an odd number of bits and a logical "1" output of the error detecting circuitry. If either or both of these conditions are violated, operation is transferred to the other memory. During regenerate or store cycles, since parity checking cannot be performed, failure detection is accomplished by the error-detection circuitry only and by parity detection during subsequent read cycles. Intermittent addressing of memory between normal cycles is also detected by the error-detecting circuitry producing a logical "1" output at the improper time. Figure 2-5 indicates the system connection of the error-detector circuits for a simplex memory.

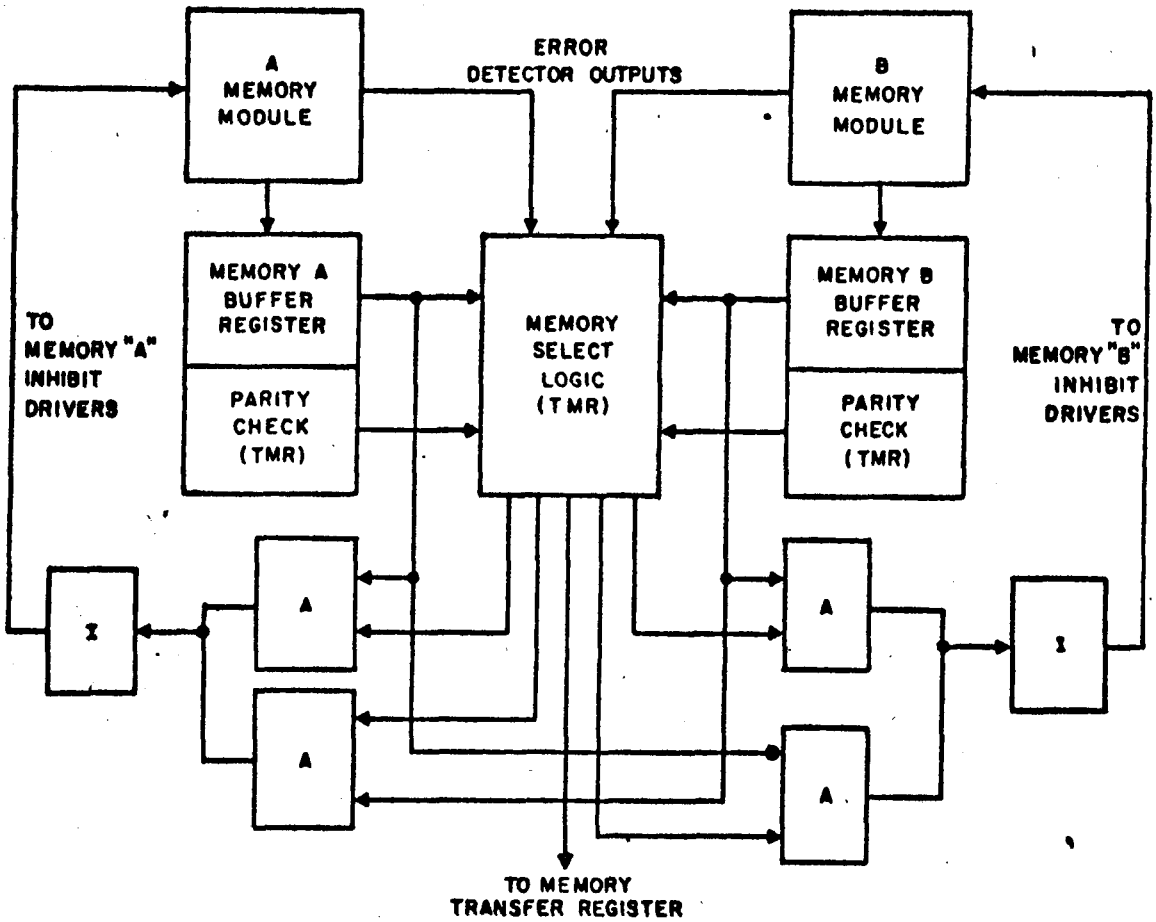


Figure 2-4. Self-Correcting Duplex-Toroid Memory System

The control latch circuits are packaged with the buffer register circuit in the computer. The output latch is in a logical "0" state for normal operation. If the error-detector output is a logical "0" at normal cycle times, or a logical "1" at the improper time, the output latch is set to the "1" state, indicating an error. Conditions resulting in an error output are as follows:

- Address without voltage source
- Address without current sync
- No address

- Dual source-single sync address
- Single source-dual sync address
- Out-of-time addressing

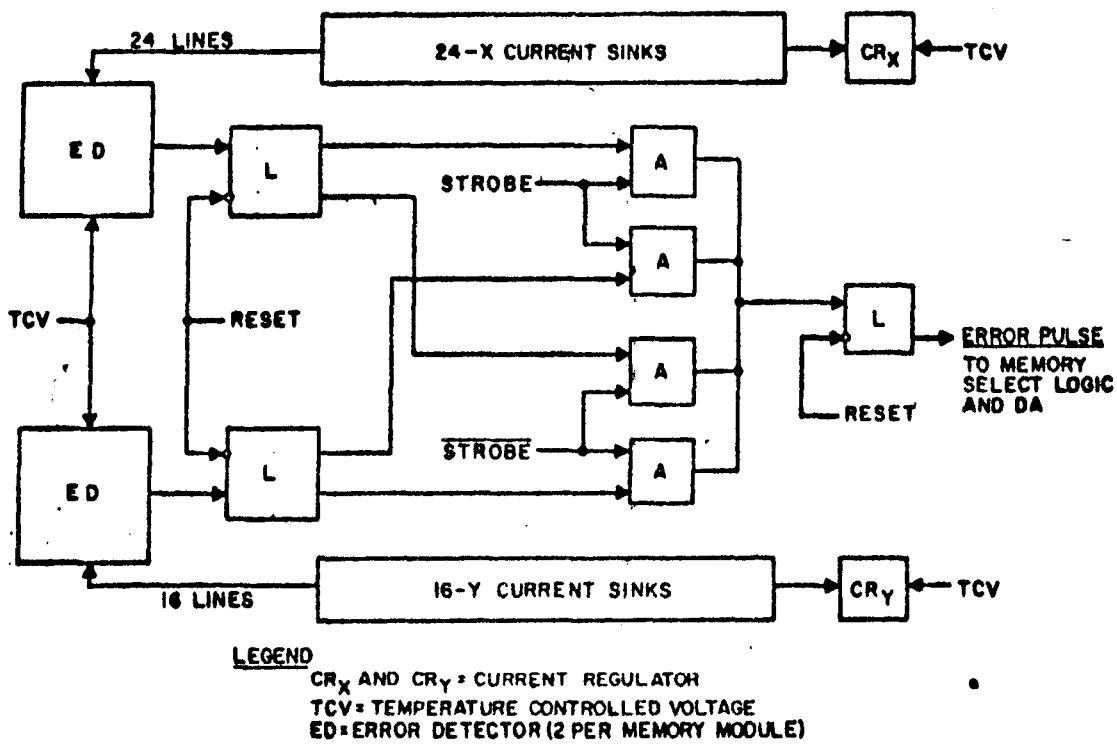


Figure 2-5. X-Y Coordinate Half-Select Current Error Detection

b. Memory Diagram

Figure 2-6 is a more detailed block diagram of a single simplex memory unit. The blocks contained within dashed lines are located in the central computer. All other functional blocks are an integral part of each simplex memory unit. Each memory consists of a 14-bit core array, which represents the two memory syllables. Instructions occupy one syllable and data occupies two syllables. The 4096 words in each syllable are divided (X and

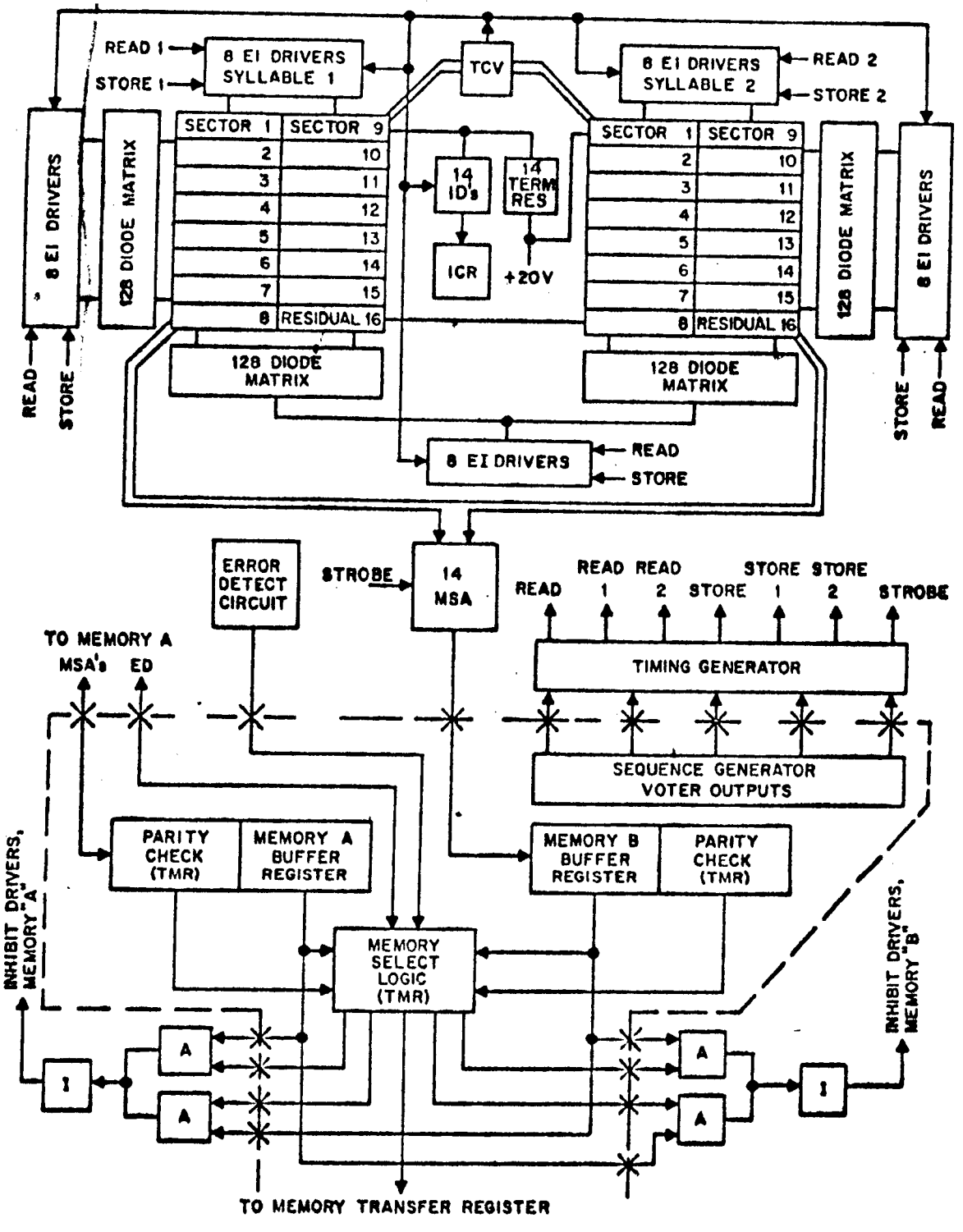


Figure 2-6. Simplex Memory Module

Y) into 16 sectors of 256 words each. Sector 16 is called residual memory. The proper choice of any of the sectors in either simplex unit is determined by the state of the data sector register or instruction sector register. Variables and most constants not associated with the polynominals or orbital check-out will be grouped together and stored in residual or data sectors.

(1) Instrumentation

Each memory array is addressed with direct-drive coincident current as shown in Figure 2-6. The appropriate X-Y coordinate memory address driver (EI) source and sink gates, and the associated diode decoupling matrices, are selected. Then the Y-coordinate address simultaneously drives both syllables with an independent X-coordinate address. Applying the Y-coordinate address before one of the X-coordinate drives occurs causes the delta noise in the nonselected syllable to decay before the selected syllable is read. Thus, the two sense lines of the two syllables can be connected in series. Therefore, only 14 memory sense amplifiers are needed instead of 28. An instruction word (13 bits plus parity) is read by addressing one of two syllables, whereas a data word (26 bits plus 2 parity bits) requires addressing of syllables 1 and 2 in sequence.

During the "store" mode, the memory buffer register controls the inhibit drivers. If "0's" are to be retained, the Y-coordinate half-select current is cancelled by inhibit current. As illustrated, each inhibit driver simultaneously inhibits both syllables through a series connection of inhibit lines for the same bit location in each syllable. As a result, each inhibit driver does the work of two.

The coordinate selection current drivers comprise a voltage source, E, and a current sink, I. Each driver is capable of either delivering or accepting current, and functions in conjunction with a like circuit in the opposite ordered group. The instrumentation of a single syllable requires only eight drivers for each order, operated in pairs, to selectively interrogate each of the 4096 word locations. During the application of the Read clock followed by Read 1 or Read 2 clocks, current is delivered from a high-order to a low-order driver. During the application of Store 1 or Store 2 clocks followed by the Store clock, current is delivered from a low-order to a high-order driver. The diode matrix in series with the address driver prevents sneak currents from passing through other nonselected address conductors, and minimizes the effects of displacement currents on current rise time caused by interwiring capacitance.

(2) Temperature Characteristics

The maximum array temperature is limited to 70°C, with a maximum temperature differential across the array of 10°C. These requirements dictate the thermal design of the memory module support structure and the location of the memory address electronics.

6. COMPUTER INPUT/OUTPUT CAPABILITY

a. General

The computer input/output capabilities are characterized by the input/output instruction and the interrupt feature. The Process Input/Output (PIO) instruction provides for transferring of a single word into or out of the accumulator or out of the memory.

The primary input/output interface will be between the computer and the data adapter. The data adapter will perform all conversion (analog-to-digital and digital-to-analog) required by the system.

b. PIO Instruction

The PIO instruction transfers data between the accumulator or memory and one-word registers and delay lines located in the data adapter or other subsystem. The operand address is used to select the desired register.

Discrete inputs and outputs can be processed by this instruction. It is possible to pack 26 discrete signals into one word. The XOR instruction will determine if any of the 26 discrete inputs have changed state. The AND instruction is used to set or reset any of the discrete outputs.

c. Interrupt

Interrupt signals can be generated within the data adapter. These signals will stop the computer program and cause a branch to a subprogram. The location of the subprogram is program-controlled and is dependent upon the HOP constant stored in a specific memory location. This subprogram will normally be used to process a block of input-output data on a periodic basis. The rate at which the timed interrupt occurs is also program-controlled and can be adjusted as dictated by the various modes of operation during a given mission.

The main program can be resumed after completion of the subprogram by executing a HOP operation from another specified memory location. This location will contain the contents of the instruction counter, sector register, and syllable latch which were stored there when the interrupt occurred.

7. LOGIC DESIGN

a. Design Improvements

Comments received from various groups during the preliminary design of the Saturn V computer have resulted in several improvements in the computer logic. Before implementing the changes, the advantages, disadvantages, impact on the computer system and the cost of implementation was carefully considered. Thus far the following changes have been implemented into the computer design:

(1) By executing a STO instruction with an address of 775, the contents of the accumulator are transferred to the PQ register. This change was deemed necessary to restore the contents of the PQ register after an interrupt subroutine. Normally it is a programming responsibity to store the contents of the accumulator and PQ register after recognizing an interrupt. This frees these respective registers to be used in the subsequent I/O interrupt subroutines. At the end of the subroutine the program must restore these registers with the original data such that the main program can be resumed. This change required ten diodes and two resistors per computer.

(2) The original computer had two module registers, one for data and one for instructions. Instructions and their data therefore could be in two different memory modules, or four different memory modules if in the duplexed mode of operation. This created problems and excessive logic for memory module switching and error detection, since the status of four memory modules must be remembered instead of just two modules. Since no requirements could be foreseen which must use both module registers, it was decided to incorporate them into one module register. By combining the two registers into a single register, both instructions and data will come from the same memory module. A saving of 104 diodes, 48 resistors and 12 transistors per computer was realized by making this change. This change does not include the additional logic required to monitor the error condition of four modules as opposed to two because the logic was not designed when the decision to eliminate one of the registers was made. Estimates of the components required to implement this logic approximate those given above.

(3) The PIO instruction was changed to permit more output addressing capability. Previously the low-order address bit determined the direction of the PIO data, i.e., A1 equal to "0" indicated an output operation, A1 equal to "1" an input operation. The change, which required two diodes, permits an input when A1 and A2 are both ones. Any other combination (except A1 and A2 both "0") is an output address. This change allows 128 input addresses and 256 output addresses.

b. Removal of Process Delay Line Instruction

The preliminary design of the data adapter indicated that the PDL (Process Delay Line) instruction could be eliminated. The PIO instruction can be used for all input-output operations. This was made possible in part by reducing the number of delay lines in the data adapter and shortening their length from 224 to 82 usec.

Elimination of the instruction and its associated logic netted a component saving of 136 diodes, 51 resistors, and 8 transistors per computer (585 total components) plus removal of 6 voter trios for a saving of 366 components. The total of components removed per TMR computer was 951.

The removal of the PDL instruction from the computer repertoire made that operation code available for some other instruction. Several candidates were immediately suggested as possible replacements, of which the following were analyzed to determine their cost of implementation:

(1) A Store Product Quotient (SPQ) instruction which would place the contents of the PQ register directly into memory. This operation presently requires two instructions. A CLA 775 will place the contents of the PQ register into the accumulator and a subsequent STO instruction will store the accumulator contents into memory. However, after an MPH instruction the product ends up in the accumulator and consequently an SPQ is not required. Implementation of the SPQ instruction requires approximately 175 components including a voter trio.

(2) An SML (Sign-Magnitude Limit) instruction for driving sign and magnitude ladder networks was considered. This instruction compares a two's complement number in the accumulator to a sign and magnitude number in the memory. If the accumulator contents are greater, the contents of the memory location would replace the accumulator contents. For this part of the operation the instruction time would be 164 usec. However, if the contents of the memory are greater, the accumulator remains unchanged and the total instruction time is 82 usec. This instruction would

require approximately 780 components, including three voter trios for implementation.

No decision has yet been reached on a replacement for the PDL instruction.

c. Logic Voter and Disagreement Detector

The Saturn computer logic has been made triple modular redundant to achieve the high reliability required. Certain logic signals within the machine have been selected to be voted on. A typical voter trio for signals used internally within the logic is shown in Figure 2-7. There are three separate voters, one for each channel of the TMR computer. Each voter of the trio provides the signal drive representing the voted output to its respective channel.

Previously, two types of voters were proposed, one of the type previously indicated and a second type voter at the interface between the computer, memory, and data adapter. This interface voter was to be "ultra-reliable" and would reduce the three TMR signals originating in the logic to a single line. An interface voter was designed using component redundancy to achieve the required voter reliability. This voter required six ULD's to implement it. Because the redundant component circuit dissipated relatively large power, the ULD area would not permit a large number of resistors to be mounted per ULD.

When it became evident that the data adapter logic interfacing with the computer was to be TMR while the memory was to operate in duplex, a decision was made to use standard logic voters at each interface. To satisfy the duplexed memory requirements, a voter duo was implemented as illustrated in Figure 2-8. Each of the duos will drive four of the memory modules, i.e., one voter circuit will drive the odd numbered memory modules and one the even numbered modules. The duplexing will be instrumented such that duplexed pairs will contain an even and an odd module. Consequently, during the duplex mode of operation both voters of the duo will be operable. Successful operation of the system, therefore, does not hinge on successful operation of a single voter circuit.

The logic signals interfacing with the data adapter were also used within the computer. Therefore these signals would have required both type of voters, an interface voter and a logic trio. Making the data adapter logic TMR eliminated the requirement for the interface voter. Consequently, the signals required can be derived from the logic trios.

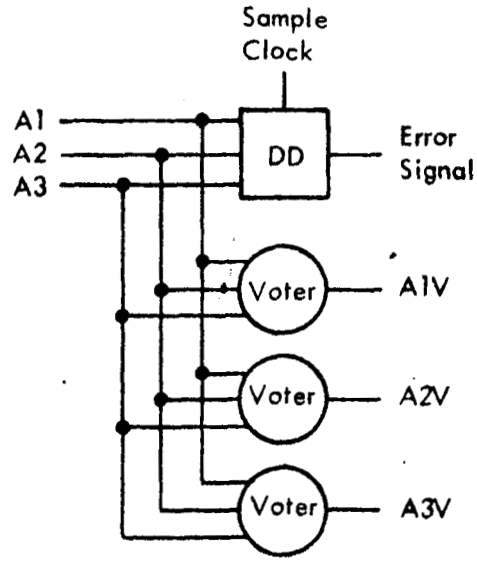


Figure 2-7. Typical Voter for TMR Computer

The resultant impact to the computer meant eliminating 15 redundant interface voters required for the data adapter (a saving of 90 ULD's), and a reduction in ULD count required for the memory interface; 45 interface voters replaced with voter duos (a saving of 135 ULD's). Therefore, the ULD count was reduced by 225 ULD's and a saving in power of approximately 8 watts was realized.

When the computer design was completed, the load on each of the computer logic signals could be accurately determined. In all but 25 cases the standard inverter output could handle the fan-out. These 25 cases were voted signals with large fan-out characteristics such as timing gates and decoded operation code signals. A special power voter was designed for these cases. This circuit is the same as the regular voter except for the final drive section.

Here the regular voter inverter (VIN) circuit is interchanged with the high-current inverter (HCI) circuit to provide the required fan-out. The VIN can drive a resistive load of four 1.5k AND's or their equivalent. The HCI can drive a resistive load of ten 1.5k AND's or their equivalent.

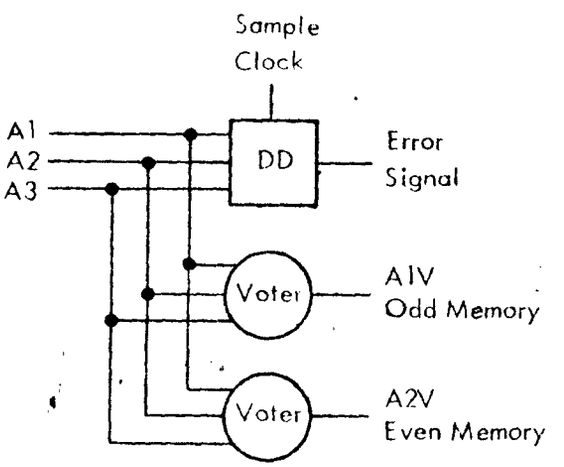


Figure 2-8. Typical Voter for Duplexed Memory Operations

As previously illustrated in Figures 2-7 and 2-8, each voter trio or duo is associated with a disagreement detector for that signal. This circuit compares the three inputs and indicates, via its output, if the inputs are identical during the sample time. The disagreement detectors are clocked to provide the sample time. The sampling period was originally assumed to follow the clock pulse which caused the input signal to change.

The computer logic, and the assignment of disagreement-detector sampling times was initially made using the above assumption. It was later observed that there could be a natural skew in the clock pulses of the three computers since each channel of the computer has its own clock generator

and clock driver circuits. Because of this allowable skew it would be possible to develop an erroneous disagreement signal. Consequently, the disagreement detectors were sampled with the second clock pulse after the clock which caused the input to change. For the majority of cases this involved changing only the clock on the disagreement detectors. In these cases the logic signals always changed on the same clock pulse or on two consecutive clock pulses. A buffer clock pulse is always available to enable the disagreement detector to be clocked with the second clock pulse after the last change.

In several instances, however, the logic signals were designed to change on three different clock pulses. For these cases the logic had to be changed to provide a safe time to clock the disagreement detectors. The following two solutions to these cases were possible:

- Change the clock pulses on the logic, where possible, to use only two consecutive clocks.

- If the first solution is impossible, make the voted signals change fast enough on the third pulse so that the fourth clock pulse can be used to clock the disagreement detectors. This latter approach can be accomplished by clocking the subject signal with a 1.25k AND resistor instead of the normally used 2.5k AND resistor.

  In the logic it was necessary to rearrange the timing of the operation code register so it now changes at clock pulses X and Y. Previously, it could change during clock pulses X, Y and Z. Similarly some of the latches in the transfer register were changed. This change could not be made to all latches in the transfer register. Some latches, i.e., transfer register positions TR1, TR6, TR9 and TR12, had to be changed on three different clock pulses. For example, the TR12 latch had to change on clock pulses X, Y and Z. By making the AND-gate resistor which was clocked at Z time a 1.25k resistor, the TR12 signal changed fast enough to allow the voter disagreement detector to be clocked at clock pulse W.

d. Logic Drawings

The preliminary logic design for 35 Saturn V computer drawings was released. These drawings were intended to represent the computer logic, placement of the voters within the logic and general memory electronics. They were subsequently used to convert the logic to actual hardware, i.e., make ULD assignments and divide the logic into MIB's for assembly into pages.

e. Voter Standardization

Since the voter pages lend themselves to standardization, the number of voter types was minimized, thereby keeping the total number of pages to a minimum. This effort resulted in three page types consisting of five MIB types (a total requirement of 15 pages). It will also result in a proportionate saving in manufacturing and testing costs will also result from this standardization. The page types are as follows:

- Type A - Three trios of high current voters and seven trios of normal voters
- Type B - Twelve trios of normal voters
- Type C - Sixteen dual normal voters (interface voters)

The 15 voters consist of nine type A's, three type B's and three type C's (a total of 174 voters). Of the 174 voters, two dual voters, four trio voters and two DDI's are not used, thereby providing spares.

f. Wire Lists

Wire lists are used to facilitate the design and fabrication of accurate back panels (channels 1, 2, and 3 are identical). The interchannel cables and the external connectors were generated for the basic TMR machine and the simplex breadboard. These lists were produced in two forms, (1) an alphabetic list of the signal nets, and (2) a page and connector list by pin number. Artwork generated from the net lists and the connector lists is used to check final layout. These lists include the hand wiring required to interconnect the TMR module of the simplex breadboard (two channels of this module are located in channel 4). Card files are being maintained and updated for each of these lists. New lists will be generated using the basic information contained in these lists for each of the breadboard and prototype machines.

g. ULD-MIB Layout Optimization

A set of sketches was prepared to reflect the initial break-up of the computer logic into ULD's. These sketches represented the ULD's as they were assigned to each MIB. No ULD pin assignments were made but the ULD position on each MIB was assigned. Data extracted from these sketches became the input to an IBM 7090 computer program which determined the ULD pin assignments. The purpose for this automated pin assignment was to select a terminal which tended to minimize the net length and induce the least number of crossovers in the subsequent printed circuit wiring. When the pin assignment was made, the 7090 program printed out the MIB wiring list.

The actual MIB artwork was manually produced from this list. The original sketches were edited to show the pin assignment, and final MIB logic drawings were prepared.

While doing the artwork for the various MIB's, it was necessary to make changes to the computer print-out of the wiring list. Accordingly, a second program was written for the IBM 1401 computer which would edit the original listings. This would eliminate a complete new 7090 run of the same data, which is costly,and might rearrange the original net lists due to the changes being made.

IBM intends to use these programs again to generate the wiring lists for the data adapter MIB's.

h. Symbol Definitions

Definitions and functional descriptions have been assigned to the mneumonic signal names. These definitions were recorded on a punched-card deck, and with the aid of a computer program an alphabetical listing was generated. The list was published as part of Specification No. 6109008 (Computer Abbreviations and Definitions).

i. MIB Drawings

MIB drawings for all the logic have been completed and are in the release cycle. The following information is provided on these drawings:

- ULD locations and interconnections
- Through-pin connections
- Edge-pin signal list
- Test-point connections

A total of 86 drawings is required.

j. Logic Simulation

The redundancy evaluation program for the IBM 7090 computes the reliability of the TMR Saturn V computer. To accomplish this, the program must have an accurate representation of the computer logic and voter placement. The input data for this program are in the form of Boolean statements written for each inverter in the computer. These statements contain essentially all the data required in another program which performs the logic

simulation. A conversion routine was written which will prepare a set of data as required by the simulation program from the input data of the redundancy evaluation program. This data must contain set and reset statements for all the latches as well as the Boolean statements.

All the logic is divided into several smaller functional pieces since it is impractical to simulate the logic of the whole computer at one time. To date, the computer timing area has been simulated. This was done to prove that the voters would provide natural synchronization of the bit-gate and phase generators of the three TMR computers. By varying the initial states of the latches, any starting conditions could be simulated, i.e., initial states of the bit-gate and phase counters when power is turned on. Results indicate that a maximum of one phase time is required to synchronize the computer timing.

A second natural output of the redundancy evaluation program is a pictorial output of the logic by inverter (Figure 2-9). A subroutine was written which shows the AND, OR, and inverter blocks. The inputs to the AND gates are indicated, and each circuit block is numbered. Every AND gate which is driven by the inverters is numbered on the inverter output. Thus, the drive required by each inverter is easily counted and the signal tracing within the computer is simplified. This is a valuable aid in writing diagnostic programs for the computer or when making changes to the logic.

8. LOGIC CIRCUITS

a. Design

Many different logic circuit techniques were evaluated before the final circuit configuration was chosen. The circuit configuration, a form of current switching-diode logic, was found to have these advantages (listed in order of importance):

- Reliability: The circuits are inherently simple and are capable of yielding large component drift allowances in a large percentage of logical applications.
- Low Power: The circuit is designed to minimize power by sacrificing only the very high speeds. Also, many of the AND resistors are clocked and, hence, need power only when they are interrogated.
- Speed: Signal voltage levels are kept as low as possible to achieve relatively high speeds without sacrificing power.

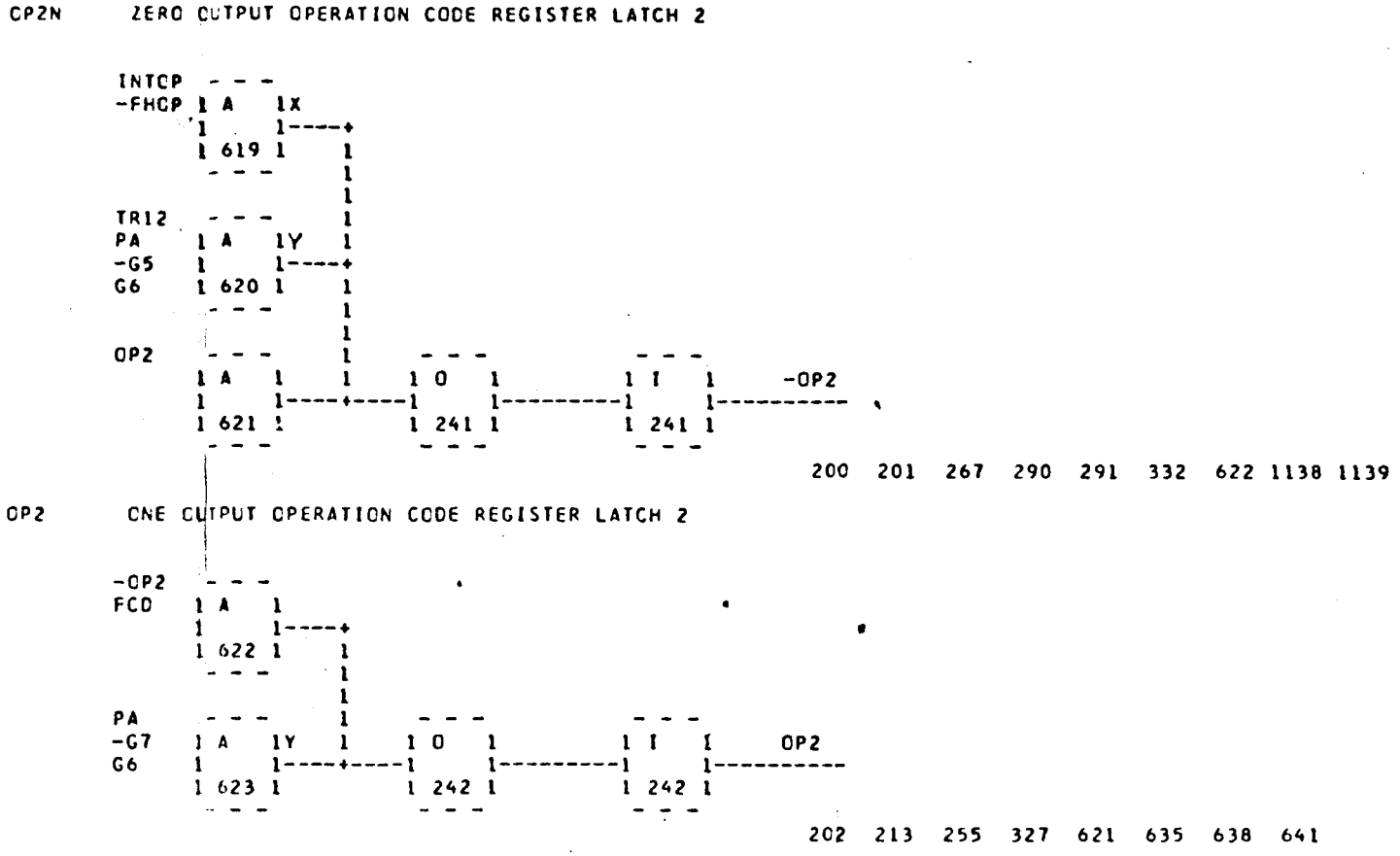


Figure 2-9. Pictorial Output of the Redundancy Evaluation Program

Most of the computer circuits use ultra-high-speed silicon planar epitaxial transistors and dual silicon planar diodes.

Simultaneous worst-case design was used for all of the circuits. This takes into account supply voltages, input responses and levels, environmental conditions, and component drift with life. The end-of-life component conditions are determined from environmental and operating life testing. Circuits are designed, where applicable, such that input signal noise, power supply noise, and output signal noise may all occur simultaneously without causing circuit failure.

A circuit was released for production only after laboratory evaluation verified performance of a circuit breadboard consisting of selected worst-case components.

The number of different circuit types used has been minimized. One standard inverter circuit serves the logical inversion function and, in conjunction with standard AND-OR diode logic circuits, is instrumented to serve as a latch, the equivalent of a flip-flop. Buffer storage circuits of the latch type have the advantages of being d-c coupled and relatively insensitive to noise. In addition, these circuit types do not have critical input signal response times.

b. Basic Logic Circuits

The basic logic circuits consist of an AND-OR-INVERT circuit family which uses diode logic and a transistor, operated in the saturated and cut-off modes. The logic circuits are designed to operate at 512 kc in a four-clock-per-bit system. The computer clocks synchronously gate logic signals by applying a 6-volt pulse to the AND resistors. Clocking the AND resistor, together with proper selection of the clock down level, allows increased capability of the inverter through time-sharing of loads and also eliminates the need for an AND diode for each clocked AND.

The logic ground rules provide that an AND may have up to ten logic inputs in addition to a clock; an OR may have up to four inputs. Since the inverter load is phased with respect to the inverter drive, there are two values available for the AND resistor. When the inverter is driven by a 2.5k AND, it may drive five 2.5k AND's or three 1.5k AND's. When the inverter is driven by a 1.5k AND, it may drive sixteen 2.5k AND's or ten 1.5k AND's. The AND loads may be a mixture of two AND resistor values where a 2.5k AND is equivalent to three-fifths of a 1.5k AND in terms of loading. The availability of two AND resistor values has the net effect of allowing one inverter to perform functions which would normally require two inverters. The inverter AND loads, in addition to being phased with respect to the drive,

may occur at different clock times and may then be time-shared. This results because an AND with its clock input in the down state presents no loading on an inverter. The principle of time-sharing may also be used to extend the number of allowable OR inputs. Also, a 2.5k AND is equivalent to half a 1.5k AND in terms of OR fan-in. Thus, the OR fan-in may be as high as eight at any one clock time.

The layout of the logic circuits was limited by basic design needs. The choice of a 0.3 inch ULD substrate dictated that only 12 of the available ULD connections could be used. The number of different types of ULD's has been minimized and all logical connective functions are satisfied with a minimum of ULD's.

Examples of the two highest usage blocks are shown in Figures 2-10 and 2-11. Figure 2-10 shows an INV module which contains an inverter with a permanently connected 1.5k AND and an extra 2.5k AND. Two INV modules are required to form a latch. The AA module of Figure 2-11 is used to obtain AND and OR diodes and AND resistors. For example, the AA module may be used to obtain two three-input 2.5k AND's with two OR diodes, a seven-input 2.5k AND with one OR diode, or just to obtain eight AND diodes. The versatility of these modules allows just two modules to satisfy all logic connections with minimum waste of unused components.

9. SPECIAL CIRCUITS

a. General

In addition to the basic logic circuits, several other special circuits are required by the computer. These circuits are associated with delay lines, timing generation, memory, and input and output functions. They are referred to as special since they are designed for a unique function, and usually have only limited usage.

Fifteen special circuit types are required. The following list indicates each circuit type and the ULD's required per circuit.

Circuit Type	ULD Type
TMR Voter	TMV-VIN (1/2)
TMR Power Voter	TMV-HCI
Delay Line Driver	DLD
Delay Line Sense Amplifier	DSA
Disagreement Detector	DD-DDI
Buffer and Oscillator	B01-B02-B03
Clock Driver	CD1-CD2-CD3-CD4-CD5-CD6

Circuit Type	ULD Type
Memory EI Driver	EI-ID2
Memory Inhibit Driver	ID1-ID2-IDT
Memory Clock Driver (MCD-1)	MCD-1-MCD-2
Memory Clock Driver (MCD-2)	MCD-3-MCD-2
Variable Delay Strobe Gate (VSG)	VSG1-VSG2-VSG3
Memory Sense Amplifier	MSA1-MSA2-MSA3-MSA4
Error Detector	ED1-ED2-ED3
Temperature Controlled Voltage Regulator (TCV)	TCV

b. Component Requirements

(1) Semiconductors

IBM conducted an evaluation to (1) improve the reliability of special circuits which use flying-lead semiconductors and (2) determine what circuit modifications would be necessary to use the leadless, glass-encapsulated chip semiconductors available from the IBM Components Division. In many cases these semiconductors could be used without changing the circuit configuration. This was accomplished by (1) special selection of critical parameters such as collector breakdown voltage (BV_{CEO}) and d-c current gain (H_{FE}), and (2) matching parameters for matched-pair transistors (V_{BE} and H_{FE}). In instances when the required semiconductor types were unobtainable from the IBM Components Division, IBM evaluated a hermetically sealed, integrated circuit package manufactured by Texas Instruments Inc.

The results of this evaluation indicated that two transistors of the same type could be contained in a six-lead hermetically sealed package measuring 0.135 by 0.260 by 0.045 inches. This would permit packaging in an area equivalent to one ULD position on MBP panels.

The following semiconductor types were evaluated and implemented into the computer and memory circuits:

Components Division Semiconductors

- Medium-speed standard-logic transistor
- Medium-speed high-voltage transistor
- Medium-speed matched-pair transistors
- Low-speed high-voltage transistor
- Medium-speed medium-high voltage transistor
- Standard-logic d-c diode

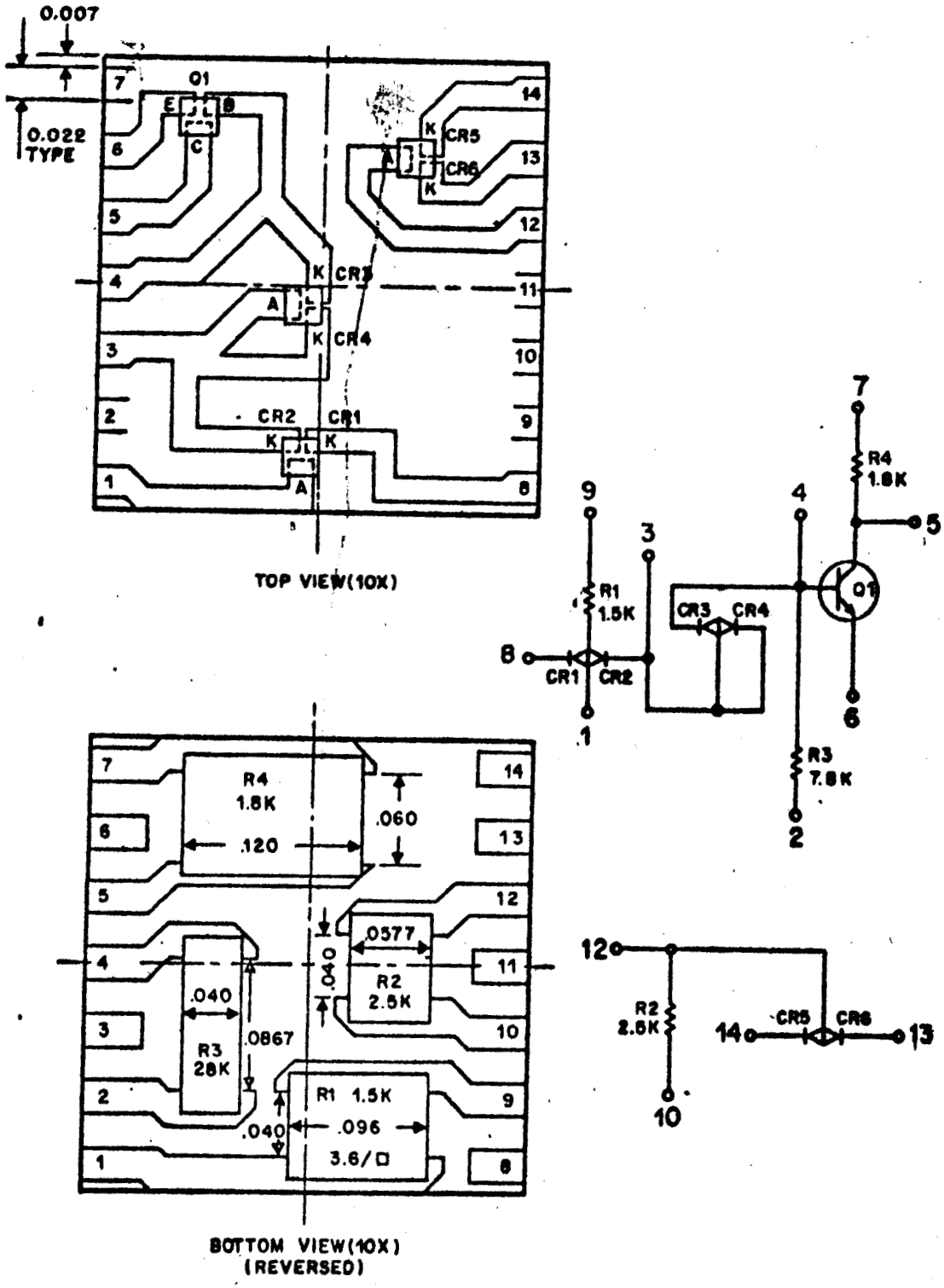


Figure 2-10. INV Module

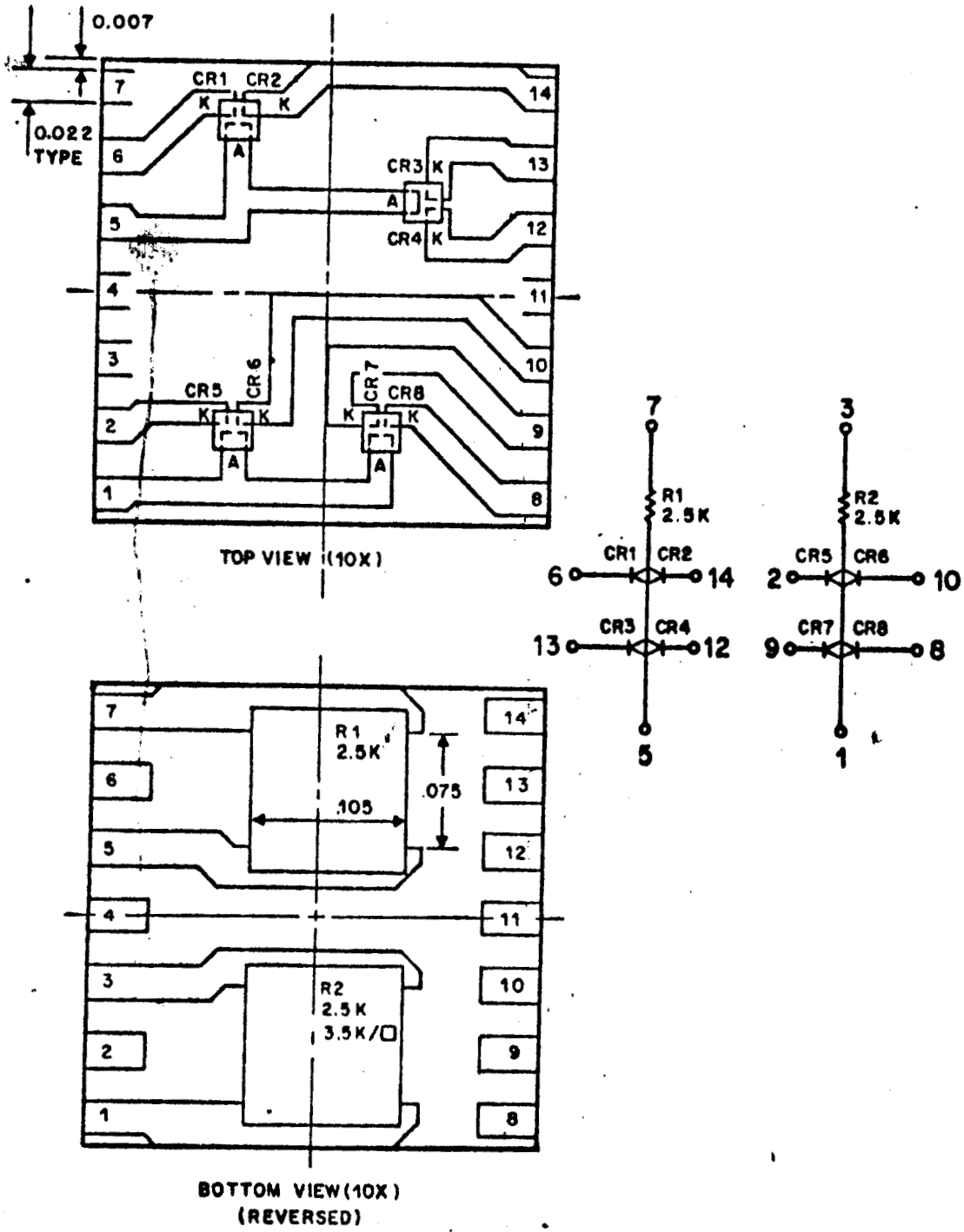


Figure 2-11. AA Module

Hermetically Sealed Dual Transistors

- Pair 2N914 NPN silicon passivated planar transistors
- Pair 2N2297 NPN silicon passivated planar transistors
- Pair TI1991 matched pair NPN transistors
- Pair 2N2412 PNP silicon passivated planar transistors

(2) Discrete Components

In certain areas of the computer and memory electronics, due to either critical tolerance requirements or packaging limitations, precision resistors, inductors, transformers, and discrete capacitors are required. In the computer, discrete components are located on the pages. In the memory modules, discrete components are located on MIB panels with ULD's and a special discrete module (Temperature-Controlled Voltage and Timing Module).

(3) Voter Circuit

A voter circuit is required to instrument TMR, and the following requirements are imposed on the voter circuit by TMR:

- The voter output must represent the majority of three inputs.
- The voter reliability must be as high as possible because of the influence of voter reliability on over-all computer reliability.
- The signal delay through the voter circuit must be small enough that the complexity of the nonredundant module is not increased when the voter is added.
- The voting circuit requires a juncture of the three module outputs. This juncture must be so constructed that a failure of one module cannot possibly affect either of the other two modules. Also, the failure of a voter component must not cause failure of a module and thus cause failure of other outputs of that module.
- The voter circuit must be capable of operating in simplex mode, in the interest of computer check-out.

The voter circuit consists of a current-summing network which is sensed by an inverter. The output of the inverter is then amplified by an additional inverter to supply an output capable of driving ten 1.5k AND's. A

power voter is also available which amplifies the inverter output to a capability of twenty 1.5k AND's. The delay through the voter circuits is less than one clock time by the amount of allowable skew between clocks of the three clock channels.

Signals between the computer and data adapter will be from voter circuits. Voter circuits have a capacitance drive capability of 320 picofarads (pf) without external dummy-load resistors. Upon review of what appeared to be a worst-case voter output from the computer, an allocation of computer, data adapter, and cable capacitances was performed. The results are shown below.

	Line Length (inches)	Capacitance (picofarads)
Computer:		
Page	3	19.2
Back Panel	14	89.5
Tape Cables	2.5	12.5
Data Adapter:		
Page	3	19.2
Back Panel	16	102.4
Tape Cables	2.5	12.5
Cable:	36	60.0
Totals	94.0	315.3

If the total capacitance is greater than 320 pf for any particular signal, a dummy-load resistor of 1.8k returned to +6V in the data adapter will increase the total allowable capacitance to 640 pf. The 1.8k resistor represents a steady-state loading equivalent of one AND on the voter circuit.

(4) Disagreement Detector

Disagreement detectors provide an output if any of the triplicated modules fail. The disagreement detector consists of a three-way exclusive OR, which is connected to each set of outputs of each trio of modules. There are approximately 200 disagreement detectors in the Saturn V Guidance Computer. The outputs of several disagreement detectors are OR'd together to provide fewer outputs to the data adapter, where a register stores disagreement detector outputs for transmission over telemetry. The inputs to the disagreement detectors are clocked to allow time for the inputs to reach steady-state conditions before sampling.

(5) Delay Line Circuits

Ultrasonic delay lines are used for short term storage. The delay medium is zero-temperature-coefficient glass. One bit of information is a 0.2 usec pulse which propagates through the delay medium at the speed of sound in the medium. Ceramic transducers are used for energy conversion. Glass delay lines provide very reliable and stable short-term storage along with simple instrumentation.

The maximum data rate of the delay line in this computer is 2.048 mc. Thus, only one delay line, delay line driver, and sense amplifier combination are required for storage of up to four different logic channels. This time-sharing of the delay line, plus driver and sense amplifier, is easily implemented by gating the driver input and sense amplifier output with the four computer clocks.

The delay line input is actually provided by the delay-line clock output of the clock generator and the delay-line driver acts only as a logic gate. This scheme helps to increase the read-out timing margin and greatly simplifies the delay-line driver circuitry.

(6) Clock Generator

The clock generator provides four sequential nonoverlapping 0.4 usec. clock pulses and the corresponding reciprocals every bit-time. The clock pulses are synchronized with the 2.048 mc signal which drives the delay-line drivers. Clock drivers provide the power gain necessary for driving up to 216 AND's on any clock output.

The clock pulses are derived by decoding the outputs of four latches driven by the 2.048 mc oscillator. Three clock generators are used in the TMR system. Voting is used as a means of automatically synchronizing the three clock generator channels when the computer is first turned on.

The clock generator also provides clock pulse signals to the data adapter. These signals must be powered by clock driver circuits in the data adapter.

10. MEMORY CIRCUITS

a. General

The basic circuits used to address the memory array have not changed greatly during this contract period. However, the following improvements

have been implemented to facilitate communication between the TMR computer electronics and the duplex memory system.

- All inputs to each memory module are derived from computer TMR voter outputs which are connected in a duo configuration. Each voter output is assigned a separate module of the memory duplex pair.

- To control the memory operation mode (simplex or duplex), sync pulses are generated separately for each memory module under control of the simplex/duplex latch. Memory modules are selected in pairs as follows:

  Memory modules 0 and 1

  Memory modules 2 and 3

  Memory modules 4 and 5

  Memory modules 6 and 7

Therefore, any module of a duplex pair which is selected for simplex operation is controlled by the appropriate sync pulses.

b. Memory Driver (EI)

The EI circuit uses a voltage-source and current-sink arrangement to provide half-select coincident current pulses to drive the X-Y coordinates of the memory array. Sixteen EI's are required to address the Y coordinate of the 64 × 128 memory array and 24 EI's are required for the X coordinate. The EI circuit provides a current pulse amplitude of 180 ±6 ma at 70°C and 260 ±6 ma at 10°C. Current-pulse accuracy is maintained by a highly accurate Temperature-Controlled Voltage Regulator which provides the base voltage on the emitter follower transistor of the EI sink. Separate clocking of the source and sink inputs ensures that the source is applied before sinking the memory drive current and is not removed until the drive current is terminated. This minimizes the effects of drive-line inductance and capacitive-displacement current on drive-current rise time. Logic gating is provided at the address input for syllable selection of X-coordinate EI drivers. This arrangement eliminates the need for special timing generation for each syllable.

c. Inhibit Driver (ID)

The ID circuits are essentially identical to the sink portion of the EI circuits. They provide a half-select current equal in magnitude to the X-Y coordinate, which cancels the effect of a half-select at the selected coordinate. When an inhibit driver is selected during a store operation, a logical "1" is inhibited, and a "0" is retained in the memory device. The amplitude of the current pulse from the ID circuit is 180 ±5 ma at 70°C and 260 ± 5 ma at 10°C. As in the EI sink, current variations with temperature are controlled by the Temperature-Controlled Voltage Regulator.

Fourteen ID circuits are required to drive the 14-plane 64 × 128 memory array. Since each inhibit drive line is used for both syllables of the memory word, the large d-c resistance of the drive line prevents direct d-c shunt termination. Inhibit-line termination is, therefore, accomplished via an a-c shunt network consisting of a 2700-pf capacitor in series with a 150-ohm resistor. Four resistors are located on ULD-type IDT. The capacitors are discrete ceramics which require an equivalent area of one ULD per capacitor.

d. Temperature-Controlled Voltage (TCV) Regulator

The TCV circuit provides a linearly changing output voltage that is a function of the average ambient temperature of the memory array. A current-temperature coefficient of -1.33 ma/°C compensation is required for half-select memory drive currents. To ensure address-pulse-current accuracy, the linearity of the TCV circuit voltage is held to within ± 0.5 percent. Dynamic regulation is held ± 10 mv over the entire range of TCV. These stringent requirements dictate that tightly controlled discrete components be used if circuit operation is to remain within the specified limits over the temperature range.

The TCV circuit consists of a current source that drives the Temperature Sensing Element (TSE) located in each memory plane and a buffer amplifier to reflect the voltage drop across the series-connected TSE resistors. The TCV circuit is capable of driving 14 Inhibit Drivers and 40 EI Drivers simultaneously.

e. Memory Clock Drivers (MCD-1 and MCD-2)

The MCD's provide the basic timing that controls the pulse width and pulse delay of the EI and ID output drive currents. An MCD-2 provides an input to the Variable Strobe Gate, which initiates a delayed pulse to activate the Memory Sense Amplifier at the proper time for reading information out of the memory. Refer to Figure 2-12.

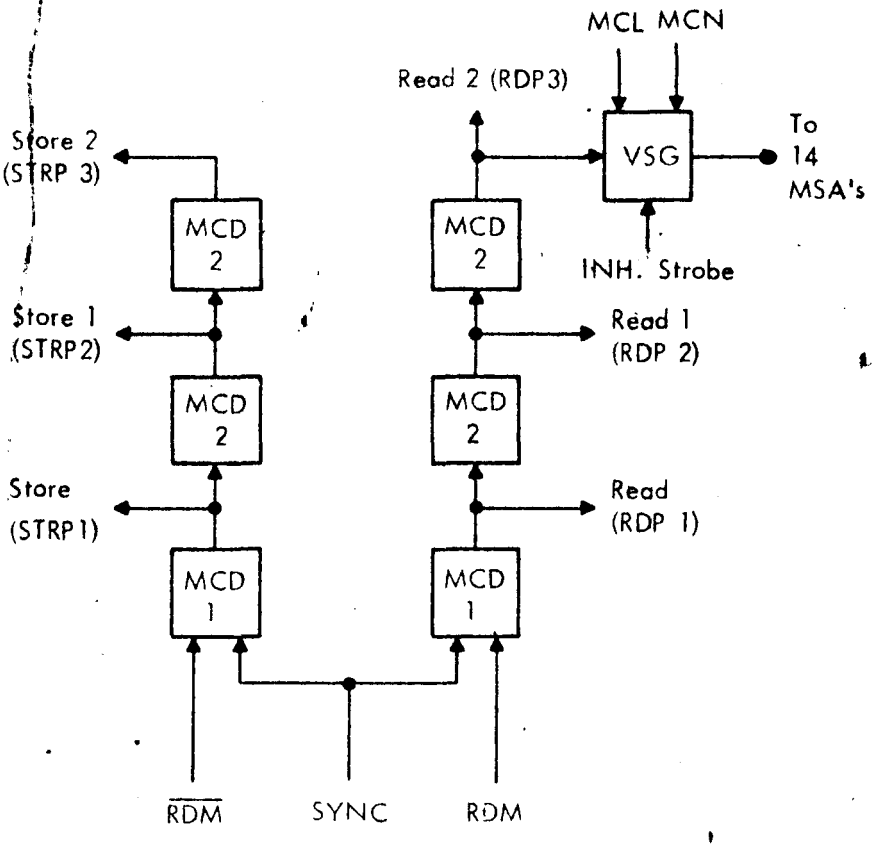


Figure 2-12. Memory Clock Drivers

When the sync pulse is received from a TMR voter output, depending upon the state of inputs RDM and $\overline{\text{RDM}}$, either a read or a store cycle is initiated. The MCD-1 provides a 3.5 usec pulse to the EI driver voltage sources and to an MCD-2 which generates a 2.5 usec pulse delayed 0.5 usec from the leading edge of the MCD-1 pulse. The 2.5 usec pulse drives the EI driver current-sinks in the Y coordinate, and 14 inhibit drivers and another MCD-2 which generates a 1.5 usec pulse delayed 0.5 usec. The 1.5 usec pulse drives the X coordinate EI driver current sinks. During the read cycle an MCD-2 provides an input to the VSG circuit.

The MCD circuits consist of emitter-follower output stages driven by pulse-width control circuitry. In addition, the MCD-2 contains a delay circuit at its input to allow alignment of the input/output pulse overlap. Precision pulse-width and delay control components are located in the TCV and timing module along with ULD's and hermetically sealed discrete transistors.

f. Variable-Strobe Gate (VSG)

The VSG provides a pulse down-level to the Memory Sense Amplifier (MSA) when the "0" response of the memory array has sufficiently diminished in amplitude so as not to activate the MSA and provide a false data output signal. The width of the VSG pulse down-level determines the width of the MSA data output whenever a "1" is read from the memory array. The delay circuit of the VSG is activated from pulses received from the MCD-2. An inhibit-strobe gate signal disables the VSG circuit during the regeneration or store cycles.

Marginal checking of memory performance is provided by generating early and delayed strobe pulses. Timing is controlled by inputs MCN and MCL which are selected by laboratory test equipment. During normal operation these inputs are open circuited to force a nominal timing condition. Early-strobe generation is performed by grounding the MCN input, and delayed-strobe by applying +6 VDC to the MCL input.

g. Memory Sense Amplifier (MSA)

The MSA circuit discriminates between "1's" and "0's" read from the memory array. Only one stage of voltage amplification is required to provide a threshold signal sufficient to trigger the output stages. A differential amplifier at the sense-line output provides common-mode noise rejection. The noise level is limited to 0.25V peak-to-peak at a frequency of 1 mc for a 10:1 signal-to-noise ratio. This amplifier is then buffered from the load by two emitter followers. The emitter followers drive a transformer in a differential mode to yield maximum voltage gain. The use of the transformer has reduced component count by eliminating the need for d-c bias stabilization.

The output of the linear amplifier circuitry is then coupled into the output-switching circuit,which is gated by a strobe input from the VSG circuitry. Since the memory array output voltage signal-amplitude and switch-time vary with temperature, a noise-free threshold is established along with a timed sample to prevent erroneous reading of "0's". A signal of sufficient amplitude to trigger the threshold circuit at strobe time causes the output latching circuit to generate a data-output pulse equal in width to that of the strobe gate. The output is therefore independent of the linear amplifier output pulse width. This results in increased sample margin.

The data output of the MSA provides a clock input to the memory buffer register rather than a logic level. This reduces the buffer-register AND-resistor power dissipation and eliminates the need for AND input diodes. Also, the effects of time-delay variations within the memory and its

associated address and sensing electronics with respect to computer clocks is minimized by providing a direct read-out of memory in the buffer register rather than a timed sampling. This also allows for the initiation of parity checking immediately after read-out.

h. Memory Error Detector (ED)

The ED circuit provides auxiliary monitoring of memory performance during the read cycle when parity checking is performed, and during regenerate or store cycles when parity checking is not possible. This is accomplished by monitoring X-Y coordinate EI driver outputs simultaneously with the common-current regulator resistor outputs (CRX and CRY) for half-select drive current detection.

The EI source outputs are monitored by connecting sensing resistors to the output of each source with the resistors commoned in a common summing network. During normal operation, since only one voltage source is selected at a time, the output level of the summing network is insufficient to trigger the input of the detection circuit. If a component failure results in the selection of two or more voltage sources simultaneously, the output level of the summing network triggers the detection circuit indicating that parallel memory drive current paths are present.

The EI current sink outputs are monitored in a similar manner by connecting sensing resistors at the output of each sink. Since the Y-coordinate high-order and low-order drivers are never clocked simultaneously, the output resistors of one high-order and one low-order driver are commoned. In the X-coordinate, sensing is provided in a similar manner except that two groups of high-order drivers are used for syllable selection. In this case, one resistor from each driver with the same address in both syllables, is commoned with a low-order driver. The outputs of the eight groups of commoned resistors (two for Y and three for X) for each coordinate are used to drive eight groups of current amplifiers which are commoned in a summing network. During normal operation, since only one current sink is selected per coordinate, the output level of the summing network is insufficient to trigger the input of the detection circuit. If a component failure results in the selection of two or more current sinks simultaneously, multiple selection of current amplifiers at the summing network raises the threshold sufficiently to trigger the detection circuit, indicating that parallel memory drive current paths are present.

To detect the condition of missing half-select drive currents, the output of the current regulator resistors CRX and CRY is monitored. During normal operation the voltage pulse across each regulator resistor is sufficient to trigger an input circuit, which has its output connected to the EI driver voltage-source summing network. A malfunction which results in a loss of voltage

across the current regulator resistor causes the threshold level of the summing network to rise in a manner similar to that caused by an EI driver voltage source failure.

During normal operation, the output of the ED circuit produces a +6V pulse (logical "1") which occurs during memory addressing. If the ED output is a logical "0" during memory address time or a logical "1" between memory cycles, an error is propogated. The output of the ED is clocked into the computer TMR error-detection logic which, along with parity-checking logic, provides the selection control of the buffer register outputs.

11. ULD TEST SPECIFICATIONS AND USAGE

Test specifications for all 39 ULD types have been released. These specifications will be the control documents used to test ULD's for the simplex breadboard computer. They will be incorporated, in part, in the ULD drawing releases which reference the general ULD procurement specification for testing prototype computer ULD's at the IBM Components Division.

The total number of ULD's used in a TMR computer system is 4383. These are broken down as to ULD type and circuit usage in Table 2-III.

12. POWER SUPPLY DECOUPLING

Power supply decoupling requirements have been established. The logic and voter channels will be filtered by capacitor pages, i.e., one capacitor page per channel. Three different types of capacitor pages are required, one for the TMR logic channels and one type for each of the two voter channels. Memory power decoupling will be provided at the central distribution panel, which interfaces with a maximum of eight memory modules. Each memory module will also contain high-frequency monolithic ceramic decoupling capacitors. All capacitors are connected in a quad configuration to eliminate a single short-or-open failure causing transients in the power distribution system.

13. SATURN V COMPUTER FINAL RELEASE DRAWING NOMENCLATURE

Table 2-IV shows assignments for final design and performance specifications, ULD Test specifications, Page and Memory Panel Test specifications, and logic drawings.

Table 2-III

ULD Data - Saturn V TMR Computer
With 4 Memory Modules

Page or Memory Panel / ULD Type	1	AA	AB	TMV	VIN	HCI	CLN	CDN	CD1	CD2	CD3	CD4	CD5	CD6	B01	B02	B03	DSA	DLD	DD	DDI	MSA1	MSA2	MSA3	MSA4	ID-1	ID-2	EI	MCD-1	MCD-2	MCD-3	VSG-1	VSG-2	VSG-3	ED-1	ED-2	ED-3	TCV-1	IDT
Oscillator and Buffer 6109254					3					13	3																												
Clock Generator 6109253	30		13	9	6			10							3	3	3																						
6-Clock Drivers 6109252							36		24	24	48	24	24	36																									
3-Timing 6109210	78	9	18																																				
3-Multiply-Divide 1 6109212	99	54	12																																				
3-Multiply-Divide 2 6109218	54	84	15																																				
3-Multiply-Divide 3 6109230	126	39	12																																				
3-Operation Code 6109213	54	27	6																																				
3-Arithmetic Unit 6109231	69	66	12																																				
3-Module Register and Timing 6109236	96	60	15																																				
3-Interrupt 6109215	45	33	12																																				
3-Sector Register and Y Decode 6109216	105	60	3																																				
3-Address Register and X Decode 6109232	144	15	6																																				
3-Memory Parity Check 6109233	114	24	12																																				
3-Transfer Register 2 6109214	105	54	9																																				
3-Transfer Register 1 6109211	81	45	18					3																															
3-Memory Error Detection and Switch 6109235	102	66	6					3																															
3-Delay Line 6109234	48						24																																
3-Voter Type A 6109242				270	108	81	53											6	6																				
3-Voter Type B 6109245				108	54															90	8																	
3-Voter Type C 6109246				96	48															36	2																	
2-Memory Buffer Register 1 6109250	40		36																	48	3																	
1-Memory Buffer Register 2 6109251	18		14																																			
6-Y Drive Memory Panel 6110340																										64	64						16	4	4			
6-X-1 Drive Memory Panel 6110350																										64	64						16	4	4			
6-X-2 Drive Memory Panel 6110360																										32	32											
12-Sense Amplifier Panel 6110370																					56	56	56	56	56	56												
6-Inhibit Panel 6110332																												8	24	16	4	4	4			8		32
6-TCV and Timing Module																																					32	
Total ULD's	1408	636	219	483	219	81	113	16	24	37	51	24	24	36	3	3	3	6	6	174	13	56	56	56	56	56	216	160	8	24	16	4	4	4	32	8	8	8	32

Total ULD's per TMR system - 3579 + 804 memory ULD's = 4383

Table 2-IV

Drawing Nomenclature

Drawing No.	Release
6110900	Reserved-Unit Assembly Drawing
6110901	Reserved-Electrical Schematic Drawing
6110902	Reserved-Mechanical Schematic Drawing
6110903	Reserved-Assembly Specification
6110904	Reserved-Test Specification
6110905	Reserved-Unit Requirement Specification
6110906	Reserved-Functional Schematic Drawing
6110907	Reserved-Design Description Drawing
6110908	Spare
6110909	Spare
6110910	AND-OR-Invert, Design and Performance Specification
6110911	TMR Voter, Design and Performance Specification
6110912	TMR Power Voter, Design and Performance Specification
6110913	Delay Line Driver, Design and Performance Specification
6110914	Delay Line Sense Amplifier, Design and Performance Specification
6110915	Clock Driver, Design and Performance Specification
6110916	Buffer and Oscillator, Design and Performance Specification
6110917	Logic Disagreement Detector, Design and Performance Specification
6110918	Memory Inhibit Driver, Design and Performance Specification
6110919	Memory EI Driver, Design and Performance Specification
6110920	Memory Sense Amplifier, Design and Performance Specification
6110921	Reserved-Electrical Assembly Drawing
6110922	Reserved-Mechanical Assembly Drawing
6110923	Memory Clock Driver 1, Design and Performance Specification
6110924	Memory Clock Driver 2, Design and Performance Specification
6110925	Variable Strobe Gate, Design and Performance Specification
6110926	Temperature Controlled Voltage Regulator, Design and Performance Specification

Table 2-IV. Drawing Nomenclature (cont)

Drawing No.	Release
6110927	Memory Error Detector, Design and Performance Specification
6110928	Spare
6110929	Spare
6110930	Clock Generator & Drivers, Logic Drawing
6110931	Bit Gate Generator, Logic Drawing
6110932	Phase Generator, Logic Drawing
6110933	Transfer Register 1-3D, Logic Drawing
6110934	Transfer Register 4-9D, Logic Drawing
6110935	Transfer Register 10-13, Logic Drawing
6110936	Transfer Register Control and Parity Logic Drawing
6110937	Arithmetic Unit 1, Logic Drawing
6110938	Arithmetic Unit 2, Logic Drawing
6110939	Multiply Divide 1, Logic Drawing
6110940	Multiply Divide 2, Logic Drawing
6110941	Multiply Divide 3, Logic Drawing
6110942	Multiply Divide 4, Logic Drawing
6110943	Multiply Divide 5, Logic Drawing
6110944	Operation Code, Logic Drawing
6110945	Address Register, Logic Drawing
6110946	Sector Registers, Logic Drawing
6110947	Module Registers and Duplex Latch, Logic Drawing
6110948	"X" Address Decode, Logic Drawing
6110949	"Y" Address Decode, Logic Drawing
6110950	Buffer Register A-1, Logic Drawing
6110951	Buffer Register A-2, Logic Drawing
6110952	Buffer Register B-1, Logic Drawing
6110953	Buffer Register B-2, Logic Drawing
6110954	Buffer Register A Parity, Logic Drawing
6110955	Buffer Register B Parity, Logic Drawing
6110956	Memory Buffer Register Selection, Logic Drawing
6110957	Interrupt, Logic Drawing
6110958	Memory Timing, Logic Drawing
6110959	Memory Sync Selection, Logic Drawing
6110960	Memory Error Detectors, Logic Drawing
6110961	Sense Amplifiers-Memory Clock Drivers, Logic Drawing
6110962	Inhibit Drivers-Even Memory Modules, Logic Drawing
6110963	Inhibit Drivers-Odd Memory Modules, Logic Drawing

Table 2-IV. Drawing Nomenclature (cont)

Drawing No.	Release
6110964	Memory Address Drivers, Logic Drawing
6110965	Page Type 6109210, Test For
6110966	Page Type 6109211, Test For
6110967	Page Type 6109212, Test For
6110968	Page Type 6109213, Test For
6110969	Page Type 6109214, Test For
6110970	Page Type 6109215, Test For
6110971	Page Type 6109216, Test For
6110972	Page Type 6109218, Test For
6110973	Page Type 6109230, Test For
6110974	Page Type 6109231, Test For
6110975	Page Type 6109232, Test For
6110976	Page Type 6109233, Test For
6110977	Page Type 6109234, Test For
6110978	Page Type 6109235, Test For
6110979	Page Type 6109236, Test For
6110980	Page Type 6109242, Test For
6110981	Page Type 6109243, Test For
6110982	Page Type 6109244, Test For
6110983	Reserved, Do Not Use
6110984	Page Type 6109245, Test For
6110985	Page Type 6109246, Test For
6110986	Page Type 6109248, Test For
6110987	Reserved, Unit Outline Drawing
6110988	Page Type 6109250, Test For
6110989	Reserved, Identification Plate Drawing
6110990	Reserved, Unit Packaging-Bill of Material
6110991	Page Type 6109251, Test For
6110992	Page Type 6109252, Test For
6110993	Page Type 6109253, Test For
6110994	Reserved, Wiring Diagram
6110995	Page Type 6109254, Test For
6110996	Page Type 6109255, Test For
6110997	Spare
6110998	Reserved, Do Not Use
6110999	Spare
6110140	ULD Type AA, Test Specification For
6110141	ULD Type AB, Test Specification For

Table 2-IV. Drawing Nomenclature (cont)

Drawing No.	Release
6110142	ULD Type INV, Test Specification For
6110143	ULD Type CLN, Test Specification For
6110144	ULD Type CDN, Test Specification For
6110145	ULD Type TMV, Test Specification For
6110146	ULD Type VIN, Test Specification For
6110147	ULD Type HCI, Test Specification For
6110148	ULD Type DD, Test Specification For
6110149	ULD Type DDI, Test Specification For
6110150	ULD Type, DLD, Test Specification For
6110151	ULD Type DSA, Test Specification For
6110152	ULD Type CD-1, Test Specification For
6110153	ULD Type CD-2, Test Specification For
6110154	ULD Type CD-3, Test Specification For
6110155	ULD Type CD-4, Test Specification For
6110156	ULD Type CD-5, Test Specification For
6110157	ULD Type CD-6, Test Specification For
6110158	Spare
6110159	ULD Type BO-1, Test Specification For
6110160	ULD Type BO-2, Test Specification For
6110161	ULD Type BO-3, Test Specification For
6110162	Spare
6110163	Spare
6110164	ULD Type MSA-1, Test Specification For
6110165	ULD Type MSA-2, Test Specification For
6110166	ULD Type MSA-3, Test Specification For
6110167	ULD Type MSA-4, Test Specification For
6110168	ULD Type IDT, Test Specification For
6110169	ULD Type ID-1, Test Specification For
6110170	ULD Type ID-2, Test Specification For
6110171	ULD Type EI, Test Specification For
6110172	ULD Type TCV, Test Specification For
6110173	ULD Type MCD-1, Test Specification For
6110174	ULD Type MCD-2, Test Specification For
6110175	ULD Type MCD-3, Test Specification For
6110176	ULD Type VSG-1, Test Specification For
6110177	ULD Type VSG-2, Test Specification For
6110178	ULD Type VSG-3, Test Specification For
6110179	ULD Type ED-1, Test Specification For

Table 2-IV. Drawing Nomenclature (cont)

Drawing No.	Release
6110180	ULD Type ED-2, Test Specification For
6110181	ULD Type ED-3, Test Specification For
6110182	Spare
6110183	Spare
6110184	Filter Capacitor Page Type 1-2-3, Test For
6110185	Filter Capacitor Page Type 4, Test For
6110186	Filter Capacitor Page Type 5, Test For
6110187	Reserved, Unit Outline Drawing
6110188	Spare
6110189	Reserved, Identification Plate Drawing
6110190	Reserved, Unit Packaging-Bill of Material
6110191	Memory Decoupling Network, Test For
6110192	Memory Diode Matrices-Termination, Test For
6110193	Memory TCU and Timing Module, Test For
6110194	Reserved, Wiring Diagram
6110195	Memory Y Drive Panel, Test For
6110196	Memory X-1 Drive Panel, Test For
6110197	Memory X-2 Drive Panel, Test For
6110198	Memory Inhibit Panel, Test For
6110199	Memory Sense Panel, Test For
6109318	Timing, MIB-A Logic Drawing
6109338	Timing, MIB-B Logic Drawing
6109348	Transfer Register 1, MIB-A Logic Drawing
6109358	Transfer Register 1, MIB-B Logic Drawing
6109368	Multiply-Divide 1, MIB-A Logic Drawing
6109378	Multiply-Divide 1, MIB-B Logic Drawing
6109388	Operation Codes, MIB-A Logic Drawing
6109418	Operation Codes, MIB-B Logic Drawing
6109438	Transfer Register 2, MIB-A Logic Drawing
6109448	Transfer Register 2, MIB-B Logic Drawing
6109458	Interrupt, MIB-A Logic Drawing
6109468	Interrupt, MIB-B Logic Drawing
6109478	Sector Register and Y Decode, MIB-A Logic Drawing
6109488	Sector Register and Y Decode, MIB-B Logic Drawing
6109518	Arithmetic Unit, MIB-A Logic Drawing
6109538	Arithmetic Unit, MIB-B Logic Drawing
6109548	Multiply-Divide 2, MIB-A Logic Drawing
6109558	Multiply-Divide 2, MIB-B Logic Drawing

Table 2-IV. Drawing Nomenclature (cont)

Drawing No.	Release
6109568	Multiply-Divide 3, MIB-A Logic Drawing
6109578	Multiply-Divide 3, MIB-B Logic Drawing
6109588	Mod. Register and Memory Timing, MIB-A Logic Drawing
6109618	Mod. Register and Memory Timing, MIB-B Logic Drawing
6109638	Address Register and X Decode, MIB-A Logic Drawing
6109648	Address Register and X Decode, MIB-B Logic Drawing
6109657	Memory Parity Check, MIB-A Logic Drawing
6109658	Memory Parity Check, MIB-B Logic Drawing
6109667	Timing and Arithmetic Voter, MIB-A Logic Drawing
6109668	Timing and Operation Code Voter, MIB-A Logic Drawing
6109669	Timing and Multiply-Divide 1 Voter, MIB-A Logic Drawing
6109677	Buffer Register 3, MIB-A, Logic Drawing
6109678	Buffer Register 3, MIB-B, Logic Drawing
6109687	Address DVR. Voter 1, MIB-A, Logic Drawing
6109688	Address DVR. Voter 2, MIB-A, Logic Drawing
6109689	Memory Timing Voter, MIB-A, Logic Drawing
6109691	Timing and Multiply-Divide 2 Voter, MIB-A, Logic Drawing
6109692	Timing Voter, MIB-A, Logic Drawing
6109693	Transfer Register Voter 2, MIB-A, Logic Drawing
6109695	Operation Codes Voter, MIB-A, Logic Drawing
6109696	Interrupt Voter, MIB-A, Logic Drawing
6109697	Multiply-Divide Voter, MIB-A, Logic Drawing
6109708	Multiply-Divide Voter, MIB-B, Logic Drawing
6109709	Buffer Register 2, MIB-B, Logic Drawing
6109717	Address DVR. Voter 1, MIB-B, Logic Drawing
6109718	Address DVR. Voter 2, MIB-B, Logic Drawing
6109719	Memory Timing Voter, MIB-B, Logic Drawing
6109737	Transfer Register Voter 1, MIB-A, Logic Drawing
6109738	Address Register Voter, MIB-A, Logic Drawing
6109739	Memory Timing and Switch Voter, MIB-A, Logic Drawing
6109747	Timing and Arithmetic Voter, MIB-B, Logic Drawing
6109748	Timing and Operation Code Voter, MIB-B, Logic Drawing
6109749	Timing and M-D1 Voter, MIB-B, Logic Drawing
6109757	Buffer Register 1, MIB-A, Logic Drawing
6109758	Buffer Register 1, MIB-B, Logic Drawing

Table 2-IV. Drawing Nomenclature (cont)

Drawing No.	Release
6109759	Buffer Register 2, MIB-A, Logic Drawing
6109768	Error Detection and Switch, MIB-A, Logic Drawing
6109778	Error Detection and Switch, MIB-B, Logic Drawing
6109788	Delay Line, MIB-A, Logic Drawing
6109791	Timing and M-D2 Voter, MIB-B, Logic Drawing
6019792	Timing Voter, MIB-B, Logic Drawing
6109793	Transfer Register Voter 1, MIB-B, Logic Drawing
6109795	Transfer Register Voter 2, MIB-B, Logic Drawing
6109796	Operation Codes Voter, MIB-B, Logic Drawing
6109797	Address Register Voter MIB-B Logic Drawing
6109798	Memory Timing and Switch Voter, MIB-B, Logic Drawing
6109799	Interrupt Voter, MIB-B, Logic Drawing
6109817	Clock Driver, MIB-A, Logic Drawing
6109818	Clock Driver, MIB-B, Logic Drawing
6109819	Clock Driver, MIB-A, Logic Drawing
6109820	Clock Driver, MIB-B, Logic Drawing
6109838	Clock Generator, MIB-A, Logic Drawing
6109848	Clock Generator, MIB-B, Logic Drawing
6109857	Capacitor 4, MIB-A, Logic Drawing
6109858	Capacitor 5, MIB-A, Logic Drawing
6109859	Capacitor 1-2-3, MIB-A, Logic Drawing
6109867	Capacitor 4, MIB-B, Logic Drawing
6109868	Capacitor 5, MIB-B, Logic Drawing
6109869	Capacitor 1-2-3, MIB-B Logic Drawing
6109878	Oscillator and Buffer, MIB-A, Logic Drawing
6109888	Oscillator and Buffer, MIB-B, Logic Drawing
6110348	Y Drive Panel, Logic Drawing
6110358	X-1 Drive Panel, Logic Drawing
6110368	X-2 Drive Panel, Logic Drawing
6110377	Sense Panel A, Logic Drawing
6110378	Sense Panel B, Logic Drawing
6110388	Inhibit Panel, Logic Drawing
6110418	TCV and Timing Module, Logic Drawing

14. DELAY LINE EVALUATION

The present Delay Line Driver configuration is an improvement over previous circuitry demonstrated in the Memory Feasibility Model. Driver delay variations have been reduced essentially to zero by directly gating the 2.048 mc square wave from the clock generator into the input transducer, dependent upon the state of the logic input at each of the four computer clock times.

The Delay Line Sense Amplifier was designed on the basis of evaluation of four delay lines purchased from Corning Glass for this specific purpose. Output characteristics were determined for single bit and two successive bit inputs.

To provide further evaluation of the delay line system, the Delay Line Evaluator which was designed and built for the Compass program was reworked to incorporate the new delay line circuits. This evaluator has a self-contained variable-frequency clock generator with enough logic to generate 15 successive input bits that are manually set with switches on the control panel. Previously, the evaluator had only the capability of recirculating these 15 bits every delay time by feeding the output of the sense amplifier back into the driver. This has been modified to allow the system to operate in the open-loop mode so that 15 manually set bits are successively entered into the delay line. This type of operation allows the operator to hunt for a worst-case bit pattern.

As a result of further evaluation with worst-case patterns it was determined that delay lines with higher-than-normal output voltages cause a marginal sample condition in the sense amplifier. This is a result of the worst-case pattern producing a voltage amplitude much smaller for the second "1" than the preceding "1".

Efforts are presently being concentrated on the elimination of pattern sensitivity of the present sense amplifier configuration. Preliminary evaluation indicates that resistive or capacitive loading of the delay line output effectively reduces the amplitude of the high-output delay lines to a level acceptable to the present configuration.

15. MEMORY CORES, PLANES AND ARRAY EVALUATION

a. Cores

The T-38 memory core planned for use in the Saturn V systems has been subjected to a critical examination during the reporting period.

The initial effort was directed toward a preliminary appraisal of ten T-38 memory cores. This effort permitted a preliminary characterization of T-38 devices over the ambient temperature range of $0^{o}C$ to $70^{o}C$. The

information obtained, while not completed, was of considerable value in establishing the general characteristics of the T-38 device. It also established the groundwork for a more elaborate test that was conducted on a 100-piece core sample.

The test on the 100-piece sample was conducted to permit a more detailed characterization of the T-38 memory device over a wide range of drive currents and temperatures. As a result of this test, detailed design information is available which describes the excitation-response characteristics of the T-38 device over the temperature range of $10^{o}C$ to $70^{o}C$.

At the outset of the test it was realized that an extended core-testing program places severe calibration requirements on the testing equipment. To minimize the effect of the variables, which exist in pulse-testing equipment, a reference core box was built. The reference core box contained three electrically stable T-38 devices. Each time the core tester was calibrated, and at frequent intervals between calibrations, the response values of the devices in the reference core box were recorded. The correlation performed during entire test on the 100-piece core sample required several weeks to complete.

As an additional effort in evaluating the T-38 device, a temperature-cycling test was performed. This test was designed to determine the effect on the response of a core which had been set to a "1" state at an ambient air temperature of $25^{o}C$, subjected to a temperature of $-20^{o}C$ for a period of one-half hour and then returned to $25^{o}C$ before being interrogated. The test was performed on a 10-piece sample and photographs of the response of each core were obtained before and after the low-temperature exposure. The results of the test indicate that the core response was not degraded when T-38 memory devices were temperature-cycled in this manner.

b. Memory Planes

Prior to the effort on the Saturn V memory planes, a trip was made to the IBM Poughkeepsie facility to examine the memory plane assembly-and-testing operations being conducted there.

The memory plane effort for the Saturn V program consisted of the fabrication and preliminary electrical evaluation of 14 planes.

Before performing the electrical tests on the planes, the plane tester was evaluated to determine the relationship between the indicated plane location responses and those at the core level. This effort included an evaluation of the error-detecting circuitry sense amplifier and current drivers. In addition, the worst-case response pattern for the plane wiring geometry was determined.

Due to scheduling requirements, the testing program had to be abbreviated. Consequently, as the planes were assembled, they were tested for open wires, correct wiring, and defective cores exhibiting catastrophic core responses. The electrical plane testing was performed at 25°C using 200 ma half-select current pulses. Data was taken on each plane identifying locations which were on the upper and lower ends of the plane response distribution. Since time did not permit the removal of cores exhibiting low "1" or high "0" responses, the location of all such devices was recorded.

The effects of various encapsulants on plane responses with respect to temperature were evaluated. Several different methods of encapsulation were tried using several different encapsulants. At this time the method that appears to yield the most promise uses Sylgard 182 applied as a conformal coating over the device matrix. Through this technique the core response exhibited less than 5 percent degradation at 10°C. The effect on core response of physically storing encapsulated planes at -20°C was also investigated. This test was performed to determine the effect on encapsulated planes that had information stored in them at 25°C and then exposed to -20°C for a 1-hour period before being interrogated at 25°C. The results of this test indicated no noticeable degradation as a consequence of the temperature cycling.

c. Memory Array

The effort to evaluate the array, which was assembled from the 14 previously tested memory planes, included electrical evaluation of the following characteristics:

- Maximum and minimum half-select address currents
- Distribution of plane responses vs half-select current amplitudes
- Array response times as a function of address current amplitudes and ambient temperature
- Storing the array at 10°C and interrogating it at 70°C
- Electrically storing the array at 70°C and interrogating it at 10°C
- Optimum current pulse amplitude compensation with temperature

The array evaluation was initiated with a test designed to yield the response distribution of the array at 70°C using maximum and minimum values of half-select address currents for this temperature. The distribution of each plane was obtained using the error-detection circuitry in

conjunction with an electronic counter. The indicated error-count for incremental slicer settings of 1 mv was then recorded. This procedure yielded a response distribution for each plane with increments of 1 mv. This test was performed at 70°C using half-select address currents of 180 and 190 ma. In addition an abbreviated test was performed using 195 ma half-select current pulses. The results of these tests indicated 180 ma to be the optimum value of half-select address currents at 70°C. This is based on the observed distribution of array responses yielding nominal amplitudes of 20 to 21 mv. The array responses appeared stable with the 190 ma half-selects but noticeable degradation of responses occurred at the 195 ma level of half-select currents. While this does not agree with the core data obtained at this temperature, a more accurate appraisal will require considerable correlation effort. Until this can be accomplished the 195 ma value yields a conservative upper limit on half-select address currents at 70°C.

After completing the previous tests at 70°C the array was evaluated at the other temperature extreme of 10°C. The criterion for array performance at this temperature was minimum address currents consistent with nominal array responses of 20 mv. It was determined that half-select address currents of 240 ma satisfied this requirement. The array was interrogated using 240 ma half-select address currents and a distribution of array responses was obtained. See Figure 2-13.

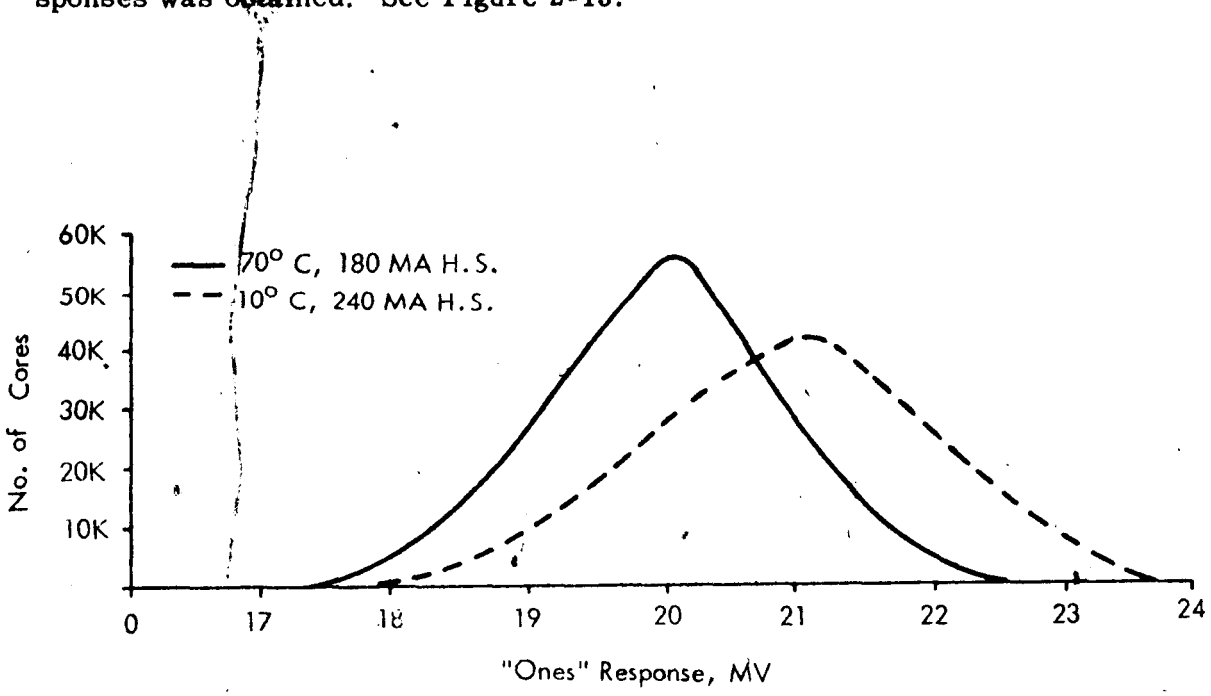


Figure 2-13. Breadboard Array Response Distribution

Additional testing was performed to determine the effects of electrically storing the plane at 10°C and interrogating it at 70°C, and then reversing the process. This test requires that a very rigid procedure be followed since after storing the array at one temperature, only a single readout can be performed at the opposite temperature extreme. The first test was performed by storing all "1's" in the array at 10°C using 240 ma half-selects. The tester was stopped and the array ambient temperature was increased to 70°C. The half-select currents were reduced to 180 ma and a single read operation was performed. The resulting array responses were photographed. This test indicated that no noticeable response degradation occurred as a result of storing the array and reading it as described.

The array was then stored at 70°C using 180 ma half-selects and read at 10°C using 240 ma. The resulting photograph of array responses indicated a degradation of approximately 30 percent in response amplitude. After an intensive investigation of this phenomenon this test was repeated using 260 ma half-selects at 10°C. The results of this test indicated that the first readout at 10°C, after storing at 70°C, yielded nominal responses of 20 mv. Subsequent responses at 10°C yielded nominal responses of 24 mv. It was, therefore, concluded that to ensure reliable operation of the array over the temperature range of 10°C to 70°C, the nominal half-select currents at 10°C should be 260 ma. See Figure 2-14.

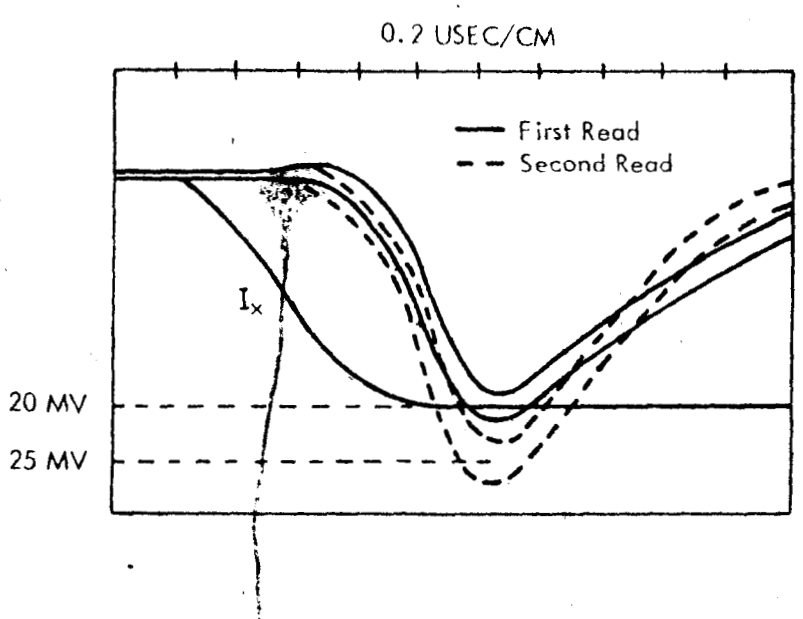


Figure 2-14. Array Response After Additional Temperature Tests

From the information obtained during the array evaluation it appears that 180 ma is the optimum value of half-select currents at 70°C and 260 ma at 10°C. This yields a half-select current compensation factor over this temperature range of 1.33 ma/°C.

B. BREADBOARD MEMORY EVALUATOR

1. FUNCTIONAL DESCRIPTION (Figure 2-15)

The memory evaluator is a test facility designed to simulate the memory operating conditions as they exist in the Saturn V computer. It uses the same logic circuits built on SMS cards rather than ULD's. For the purpose of evaluation, the timing and the memory cycle are identical to that of the Saturn V computer. The memory evaluator performs only read, store, and error-detect; no arithmetic operations take place.

In normal operation the address counter sequentially addresses each memory location, and an instruction cycle takes place at each. An instruction cycle consists of a read operation during phase A (syllable 0 or 1 as selected by the "SYL. SEL. A" switch) and a read or store operation in phase B syllable 0 and phase C syllable 1. During a store, the word being stored is that which is contained in the data switches DSW1-DSW26.

A particular address may be selected by setting the desired address in the "SET ADDRESS" switches and the "FORCE ADDRESS" switch to "FORCE ADDRESS." In this mode the same memory address location is cycled continuously.

Single-step operation is provided whereby the instruction cycles are caused to take place in discrete steps. Each cycle is initiated by a resync. In this mode it is possible to operate in particular addresses by use of the address switches or to sequentially cycle the memory array as in normal operation.

Both parity and half-select current monitor circuits are included for error detection. An error causes a nonoperate condition and causes the following to be displayed on the front control panel:

- The contents of the buffer register, including the parity bit
- The syllable in which the error was detected
- The type of error
- The address at which the error occurred

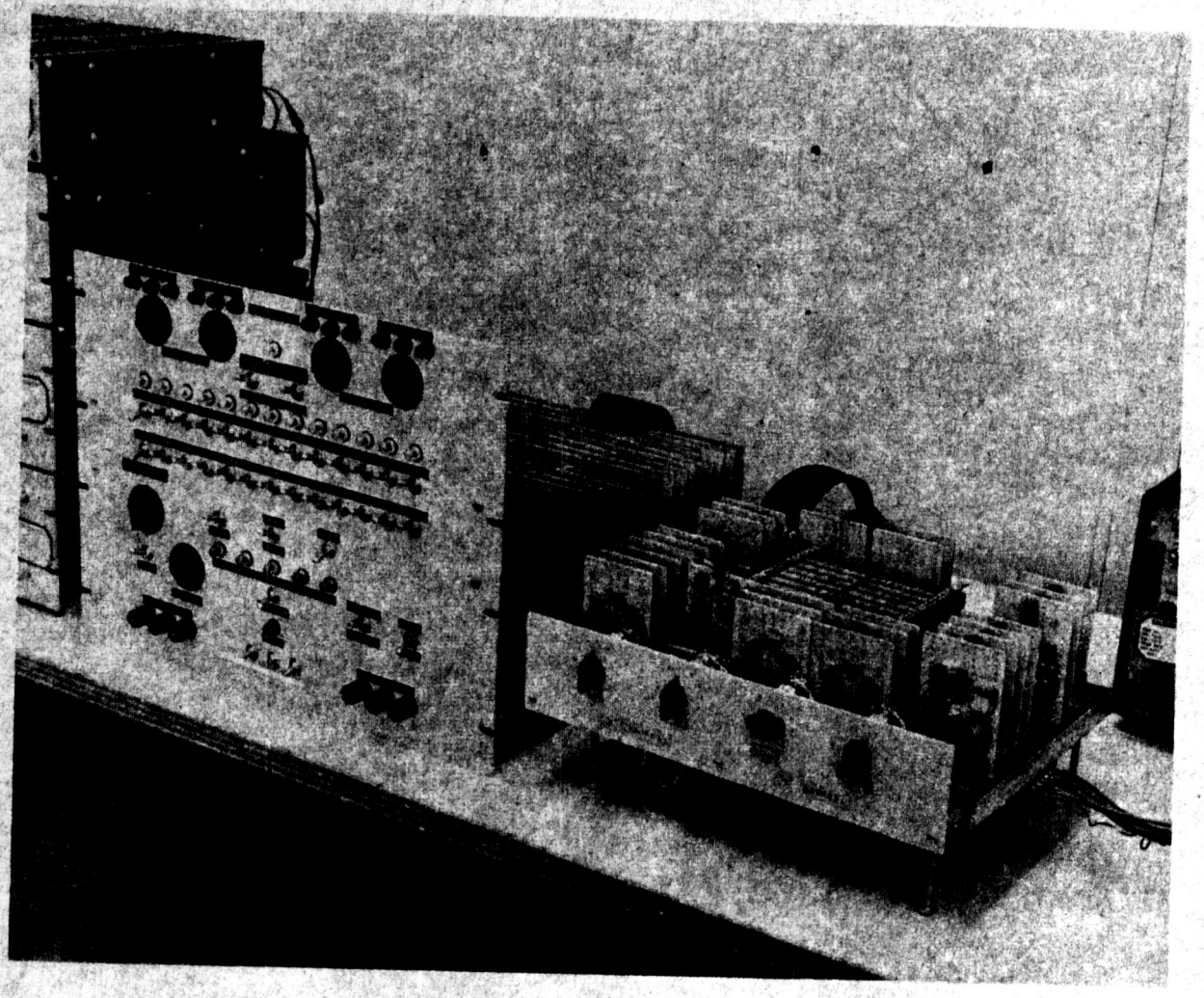


Figure 2-15. Memory Evaluator

Operation may continue and the error circuits may be cleared by resyncing. An override is provided which permits operation even though an error is present. This is the "BLOCK ERROR" switch. This override in conjunction with the "SYLLABLE-SELECT BC" and the "HOLD-ADDRESS" switches provides a convenient means of troubleshooting errors. The "SYLLABLE SELECT" switch for phases B and C has three modes:

- Normal - syllable 0 in phase B and syllable 1 in phase C
- Both B and C in syllable 0
- Both B and C in syllable 1

The "HOLD ADDRESS" switch prevents advancing the address counter. Thus, operation continues in the same address.

2. OPERATIONAL SEQUENCE

The following summary describes the control panel for implementing the above functions.

a. Turn On

(1) "RUN/RESYNC" switch to "RESYNC"

(2) Power switch to "ON"

(3) Depress "LIGHT CHECK" switch to test bulbs

b. Load Memory

(1) All locations with same information

(a) "READ/STORE" switch to "STORE"

(b) DSW1-26 to desired word

(c) "RUN/RESYNC" switch to "RUN"

(2) A Specific Location

(a) "READ/STORE" switch to "STORE"

(b) DSW1-26 to desired word

(c) "SET ADDRESS" switches to desired address

(d) "FORCE ADDRESS" switch to "FORCE ADDRESS"

(e) "RUN/RESYNC" switch to "RUN"

(3) Successive Locations with Changing Data

(a) "READ/STORE" switch to "STORE"

(b) DSW1-26 to desired word

(c) "SET ADDRESS" switches to initial address

(d) "FORCE ADDRESS" switch to "FORCE ADDRESS"

(e) "CONTINUOUS/SINGLE-STEP" switch to "SINGLE-STEP"

(f) "RUN/RESYNC" switch to "RUN" and return to "RESYNC"

(g) "FORCE ADDRESS" switch to "NORMAL"

(h) DSW1-26 to next word

(i) "RUN/RESYNC" switch to "RUN" and return to "RESYNC"

(j) Repeat (h) and (i) for successive words

c. Read Memory

Same as load except set "READ/STORE" switch to "READ" and disregard DSW1-26.

d. Error Check-Out

(1) Transients - Resync and continue

(2) Repetitive read-out of faulty location

(a) "HOLD ADDRESS" switch to "HOLD ADDRESS"

(b) "RUN/RESYNC" switch to "RESYNC"

(c) "SYL. SEL. A" and "SYL. SEL. BC" switches to indicate syllable

(d) "BLOCK ERROR" switch to "BLOCK ERROR"

(e) "RUN/RESYNC" switch to "RUN"

3. PRELIMINARY TEST RESULTS

Initial check-out of the memory evaluator using the 64 × 128 breadboard memory array began on 9 September 1963. All memory instrumentation including correct error-detection and parity-checking logic operated successfully. Preliminary observations during initial check-out are as follows:

- Nominal X half-select drive current rise time of 0.2 usec.
- Nominal Y half-select drive current rise time of 0.15 usec.
- Address lines appear to be properly terminated. No severe overshoot is present on drive currents.
- Memory operates without error except for a few catastrophic locations at + 25°C with nominal 200 ma drives and a 100 nsec marginal-check sense-amplifier-strobe time variation. Only two planes are presently being interrogated, one for data, the other for parity check.

An evaluation of memory array capacitive displacement currents in the X and Y sense and inhibit address lines has been initiated. A thorough understanding of these displacement currents is necessary to determine drive current rise time limitations and sense output time delay variations.

C. MECHANICAL DESIGN AND FABRICATION

1. BREADBOARD COMPUTER

a. General

The breadboard computer design is electrically similar to a nonredundant version of the prototype Saturn V Guidance Computer. However, the breadboard has several mechanical features which will facilitate electrical check-out and change activity.

The general breadboard computer layout is shown in Figure 2-16. The logic section includes three major subassemblies (channels). Each channel contains a number of pluggable units (pages) connected to a single back panel. There are 42 pages in the logic section: 18 in channel 1, 12 in channel 4, and 12 in channel 5.

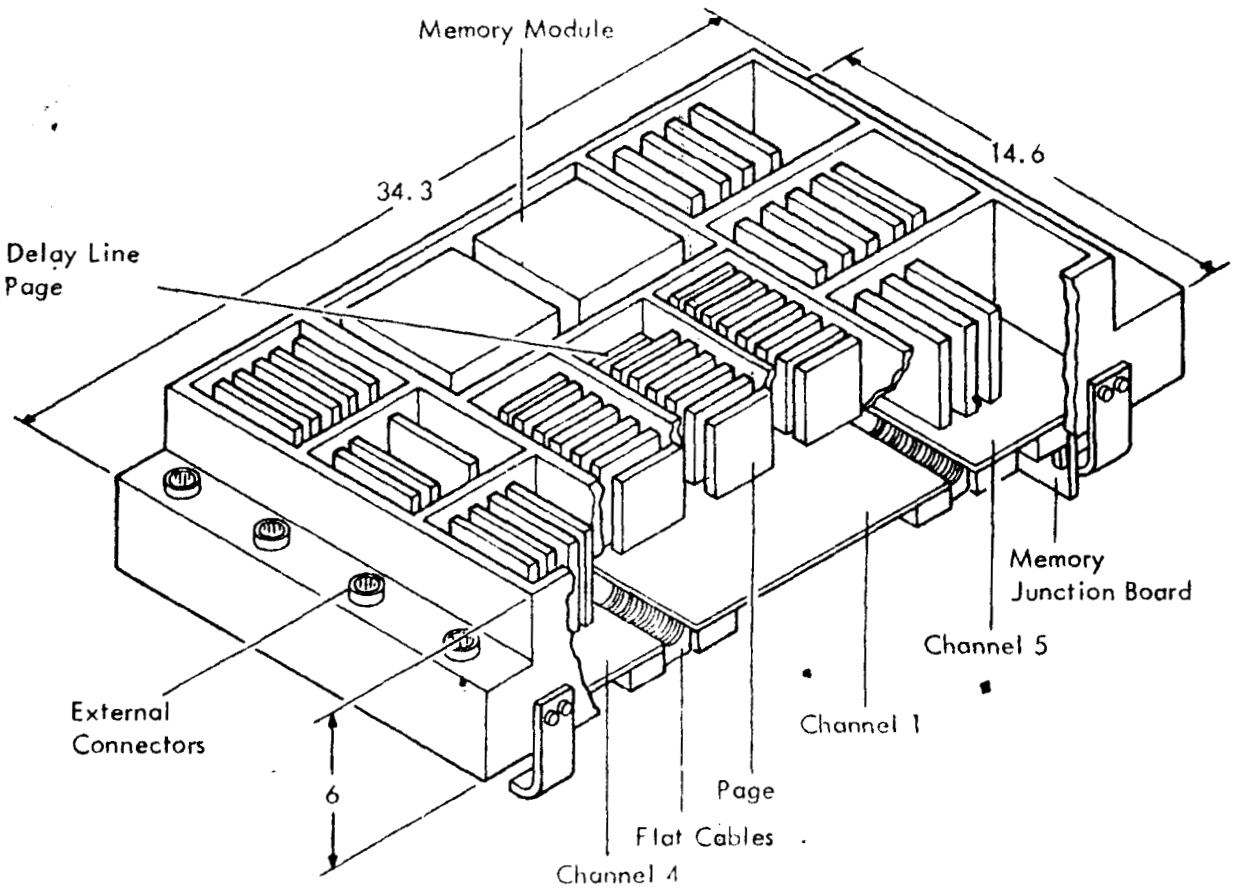


Figure 2-16. Breadboard Computer

The breadboard channels correspond to three of the five channels which make up a full-redundant computer. Channels 2 and 3 are not included in the breadboard because they would be redundant replicas of channel 1.

Initially, the breadboard will contain one 4096-word memory. Electronics, interconnections, and structural supports will be provided for later addition of a second memory module.

Breadboard computer back panels are interconnected by attaching etched flat cables to terminal blocks on the edges of the back panels. Similar flat cables will connect channels 4 and 5 to Bendix pygmy connectors used for computer input and output connections. Also, flat cables will connect the memory to channel 5. Connections common to both memory modules will be distributed by a junction board.

b. Page Design

The page (Figure 2-17) is a pluggable unit containing up to 70 ULD's attached to the outer surfaces of two multilayer interconnection boards (MIB's) sandwiched over a metal frame. The MIB's are bonded to the magnesium-lithium frame with an epoxy-impregnated, glass-fabric adhesive layer which also serves as an electrical insulator. A 98-pin connector is attached to the bottom edge of the page, and connector terminals are soldered in plated holes on the edges of the MIB's.

The 30 feed-through connections between the two MIB's at the upper edge of the page are made through teflon-insulated terminals, pressed into holes in the frame before the MIB's are bonded. The feed-through and connector terminals are soldered after the MIB's are cemented in place.

ULD's are attached to the page by reflowing solder previously applied to ULD's and MIB's. After assembly and test a thin conformal coating is applied to the page.

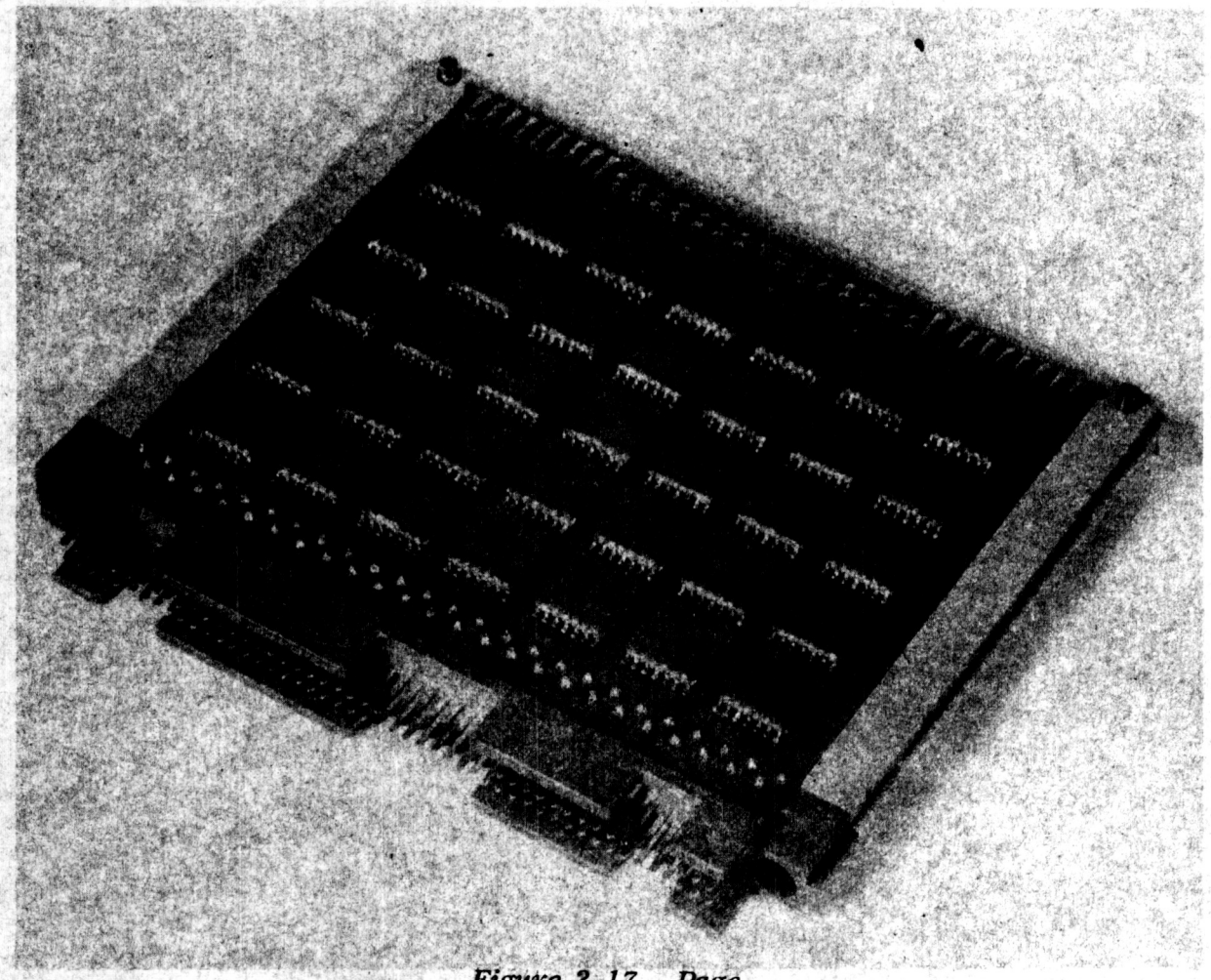


Figure 2-17. Page

Variations of the standard page are required in several parts of the computer. They include:

- The delay line page, which contains a MIB with ULD's on one side and two glass delay lines on the other side. Two brackets attached to the frame support the additional weight. A mock-up of the delay line page is shown in Figure 2-18.
- The crystal oscillator page, which contains a combination of ULD's, conventional components, and a quartz crystal.
- The capacitor page. Power supply decoupling in the logic section is accomplished in each channel by a page containing an array of microminiature tantalum and ceramic capacitors. These are attached to the page in a manner similar to ULD attachment.

c. Page Support Mechanism

The page support mechanism in the breadboard computer comprises a connector with guide pins and sockets, and tabs on the upper edge of the page frame which engage slots in the computer structure when the page is inserted. The page is held down by a rubber pad pressed against the top

Figure 2-18. Delay Line Page

edge of the frame. Metal clips on the support structure grip two edges of the page frame to provide a heat transfer path. Since the breadboard will be operated only at room temperatures, the structure will not be liquid cooled. If convection and conduction cooling are inadequate, forced air will be supplied.

The production area now has 90 percent of the required page hardware and support mechanism parts.

d. Page Connector

Since connectors compatible with page size and connection density were not commercially available, the Cannon Electric Co. and the Burndy Corp. were asked to cooperate in developing suitable connectors. Two sources were asked to reduce the possibility of delaying the program because of production problems with this critical item. Designs were coordinated so that either firm's connectors can be used on the page without modification. The Cannon connector was designed around their Micro-D twist-pin contacts. The Burndy connector uses a newly developed blade and leaf-spring contact.

Burndy has delivered 70 pairs of connectors, which are now being inspected. The remainder of their production order is due shortly. The Burndy plug and receptacle are shown in Figure 2-19. Cannon delivered a number of receptacles, but these connectors were rejected because they did not meet dimensional specifications. Cannon is now considering alternate connector body materials.

e. ULD Design

(1) Module Design

During the reporting period, the electrical designs for the computer logic, timing, and memory circuits were being translated into workable ULD topologies. Module designs were also initiated for the portions of the data adapter circuitry which will be packaged on ULD's.

Thirty-nine ULD designs, which package the bulk of the simplex computer electronic circuitry, were designed and released to production. A summary of the ULD types and quantities required for a simplex computer with a single memory unit is given in Table 2-V. A finished ULD intended for use in the simplex breadboard computer is shown in Figure 2-20.

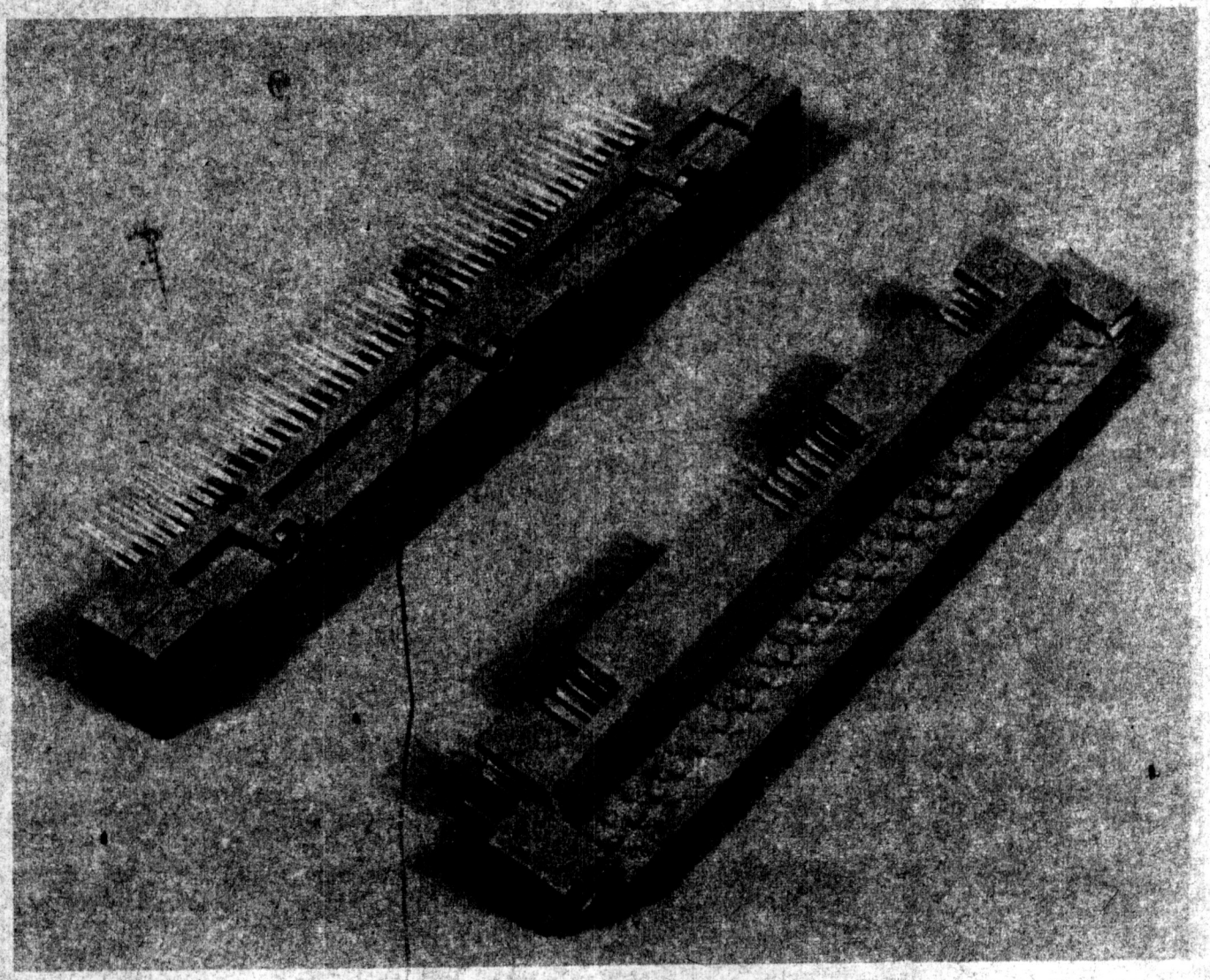


Figure 2-19. Page Connector

Table 2-V

Simplex Computer ULD Modules

Module Type	Circuit	IBM Dwg. No.	Quantity
AA	AND Extender, Logic	6109130	256
AB	AND Extender, Logic	6109131	98
INV	Inverter, Logic	6109132	545
CLN	Collector Load Network	6109133	42
CDN	Collector Divider Network	6109134	11
TMV	Triple Modular Redundant Voter	6109135	213
VIN	Voter, Inverter	6109136	94
HCI	High-Current Inverter, TMR Power Voter	6109137	41
DD	Disagreement Detector	6109138	7
DDI	Disagreement Detector, Inverter	6109139	1
DLD	Delay Line Driver	6109140	2
DSA	Delay Line Sense Amplifier	6109141	2
CD-1	Clock Driver	6109142	4
CD-2	Clock Driver	6109143	17
CD-3	Clock Driver	6109144	11
CD-4	Clock Driver	6109145	4
CD-5	Clock Driver	6109146	4
CD-6	Clock Driver	6109147	6
BO-1	Buffer and Oscillator	6109149	3
BO-2	Buffer and Oscillator	6109150	3

Table 2-V. Simplex Computer ULD Modules (cont)

Module Type	Circuit	IBM Dwg. No.	Quantity
BO-3	Buffer and Oscillator	6109151	3
MSA-1	Memory Sense Amplifier	6109154	14
MSA-2	Memory Sense Amplifier	6109155	14
MSA-3	Memory Sense Amplifier	6109156	14
MSA-4	Memory Sense Amplifier	6109157	14
IDT	Inhibit Driver Termination	6109158	8
ID-1	Inhibit Driver	6109159	14
ID-2	Inhibit Driver	6109160	54
EI	Memory EI Driver	6109161	40
MCD-1	Memory Clock Driver	6109163	2
MCD-2	Memory Clock Driver	6109164	6
MCD-3	Memory Clock Driver	6109165	4
VSG-1	Variable Delay Strobe Gate	6109166	1
VSG-2	Variable Delay Strobe Gate	6109167	1
VSG-3	Variable Delay Strobe Gate	6109168	1
ED-1	Error Detector	6109169	8
ED-2	Error Detector	6109170	2
ED-3	Error Detector	6109171	2
TCV	Temperature Controlled Voltage Regulator	6109172	2
		Total ULD's	1568

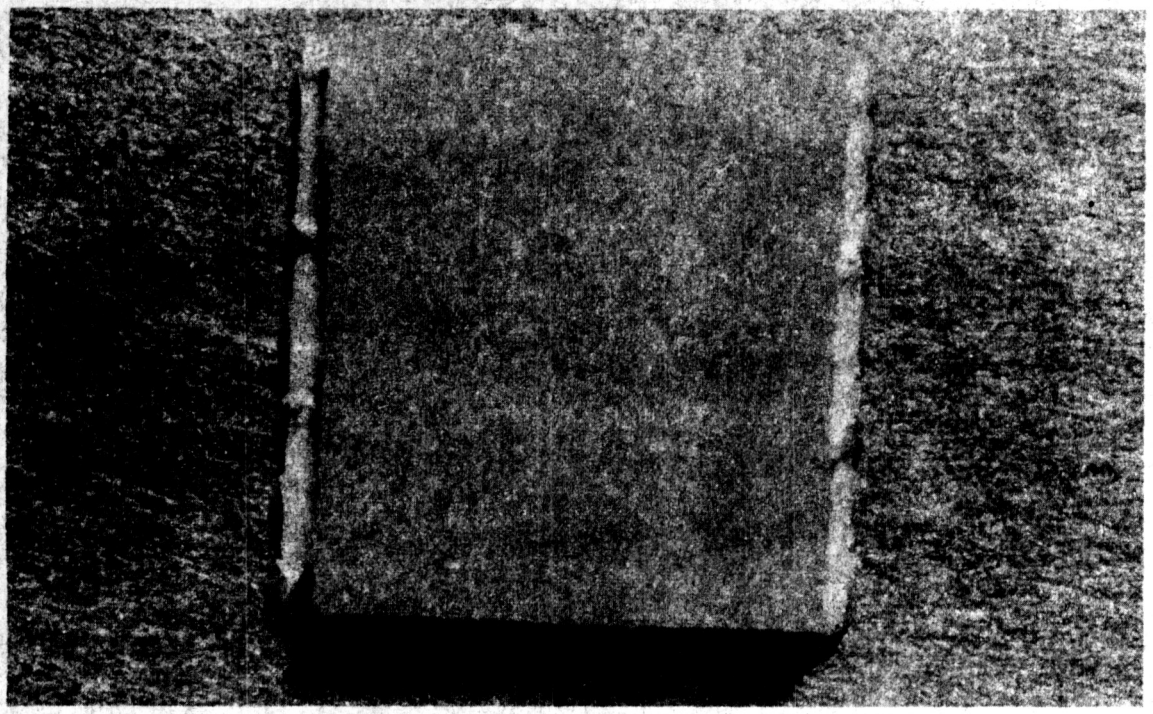


Figure 2-20. Typical ULD for Simplex Breadboard Model

Some breadboard circuits require semiconductors not currently available in a form factor compatible with the latest ULD technology. These circuits will be packaged through use of commercially available flat-packs which contain two transistors each. These hermetically sealed flat-packs will be mounted on the interconnecting circuit board with the same solder reflow technique used to mount ULD's. An example of a reflow-mounted flat-pack is shown in Figure 2-21. The flat-packs will be mounted adjacent to the ULD's which contain the remainder of the circuit.

Circuits requiring components or component tolerances which are impractical to implement with either ULD's or flat-packs will be packaged in modules of cordwood construction (Figure 2-22).

The module design was accomplished by first developing initial ULD designs for approval by the logic and circuit design groups. Following approval, 20 times size resistor and conductor layouts were drawn directly on standardized ULD form drawings. A stencil film was made from these drawings, which, when later completed with the necessary individual ULD information, served as the production ULD assembly drawings.

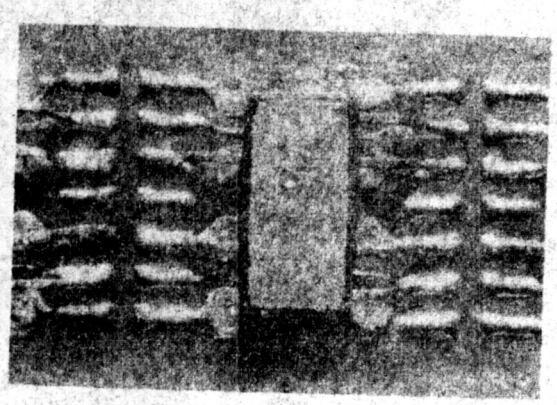


Figure 2-21. Flat Pack Containing Two Transistors Mounted to MIB by Solder Reflow

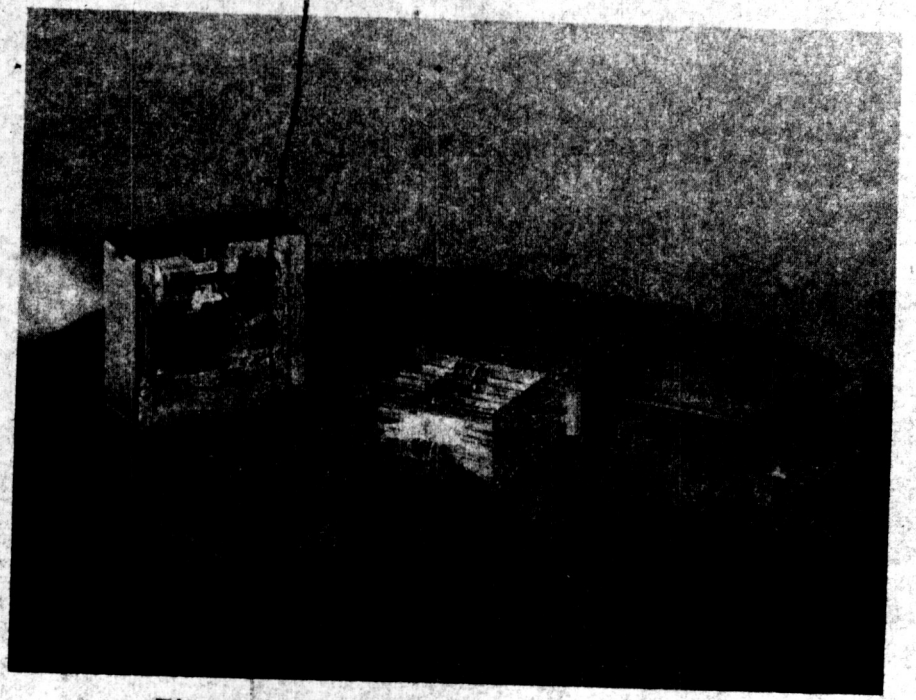


Figure 2-22. Cordwood Circuit Module

The use of 20 times size artwork masters containing all repetitious details, such as screen alignment targets, wrap-around conductor spacings, etc., was further refined to obtain the artwork accuracy required for leadless semiconductors, as well as to minimize the time between initial ULD design and final drawing release. Accuracy was assured by the utilization of a 20 times size, machine-scribed glass master, from which approximately 120 artwork masters were photographically reproduced. Both the ULD form drawings and the artwork masters contain a 0.005-inch grid system that establishes a simple, direct technique for defining all points on the ULD topology. Hence, use of the more conventional but time-consuming coordinate system of dimensioning is not required.

All simplex ULD drawings, together with the required components and materials, were released by established engineering procedures. These items will be continually updated to reflect all change activity necessitated by circuit changes, ULD improvement, and/or process requirements.

(2) Substrates

Prior to production of simplex ULD's, all ULD substrates were fabricated from Alsimag 614 alumina ceramic produced by the American Lava Corp. Although this material possessed a higher modulus of rupture and a better finish than other alumina materials, the close quality control required for simplex substrates revealed processing problems with the Alsimag 614: at first, the Alsimag 614 substrates did not meet all dimensional requirements established for simplex substrates. The vendor overcame this problem by modifying the substrate processing. But when additional parts with the correct dimensional requirements were received, a large percentage were found to have sharp edges with excessive chipping and crazing, i.e., a multiplicity of microscopic cracks. Crazing was found to be a latent type of defect which led to additional chipping during subsequent cleaning and processing steps. A second process change by the vendor to correct this condition resulted in substrates with sharp edges and a lower modulus of rupture. Investigations by Materials Engineering revealed that the sharp edges caused an undesirable thinning of the wrap-around conductors where they passed over the substrate edges. The details leading up to these investigations are now described.

Because of the 20 to 25 percent processing shrinkage for Alsimag 614, the vendor did not think it feasible to produce the substrates by cold-pressing and then firing. (The initial process was to stamp substrates from unfired sheets of the correct thickness and then fire the resulting blanks. This permitted good control of thickness and surface finish, but created difficulties in maintaining the over-all dimensions and voids on the narrow edges.)

Therefore, a second approach was tried, which was to diamond-wheel-cut the substrates from fired sheets of the correct thickness, thereby overcoming the dimensional problem, but this resulted in a chipped and crazed edge condition. The final attempt was to grind substrates to size either from oversize blanks cut as above, or from oversize cold-pressed and fired blanks. These were the substrates subsequently found to have sharp edges and to be below the minimum modulus of rupture specifications. These faults were due to a stress condition caused by the additional processing steps.

Since the Alsimag 614 could not be used for simplex substrates, the IBM Space Guidance Center requested the IBM Components Division to produce substrates of high alumina content by the cold-pressing process. Initial samples had a modulus of rupture below the minimum for Alsimag 614 and a surface finish on the order of 30 microinches. Subsequent improvements in the processing resulted in substrates which met the original simplex requirements except for surface finish and a 1 percent lower (93 percent minimum as compared with 94 percent minimum for Alsimag 614) alumina content than specified.

Materials Engineering then studied the effects of the IBM substrate surface finish on resistor properties and the adhesion of Pt-Au conductors; no noticeable effects were found. In addition, the wrap-around conductors were improved because of the absence of sharp edges. The various cleaning procedures for these substrates were also evaluated by Materials Engineering. None of the cleaning cycles used in production adversely affected the substrate; however, extended exposure to the nitric acid cleaning cycle, i.e., 24-hour immersion reduced the modulus of rupture.

After the above information and test results were evaluated, the IBM Components Division substrates were chosen for use in all simplex ULD's.

(3) Semiconductors

The decision to utilize the IBM leadless semiconductor devices in all ULD's intended for the simplex breadboard and following computers was disclosed during the last reporting period. The leadless devices replace the wire or "flying-lead" components employed during the early phases of the Saturn V program. ULD's which employ leadless and wire-lead semiconductors are shown in Figures 2-23 and 2-24, respectively.

The wire-lead devices were replaced primarily to take advantage of a potential increase in ULD reliability. The leadless semiconductors will leave little effect on component density when they are used with ULD topologies. This is primarily due to the elimination of the diode matrix ULD, which required common-cathode diode pairs not available in leadless devices.

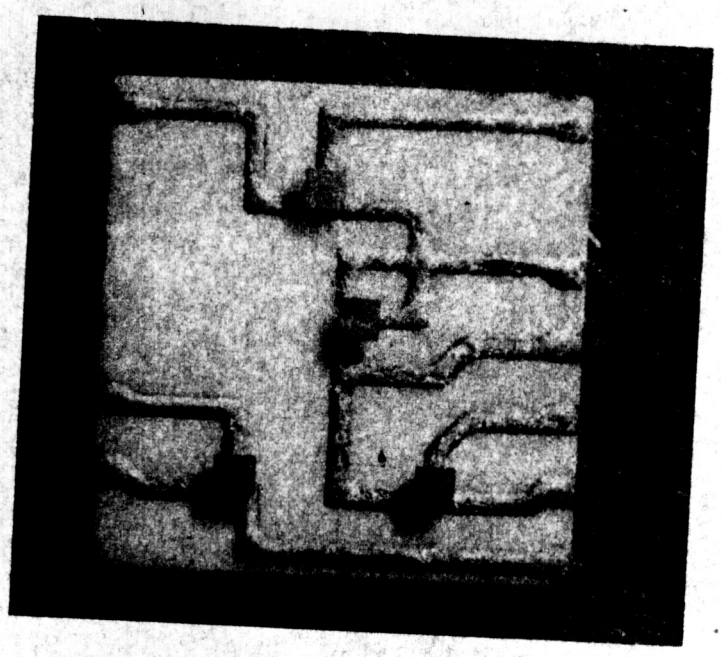


Figure 2-23. Leadless Semiconductor Devices Mounted to ULD Conductors

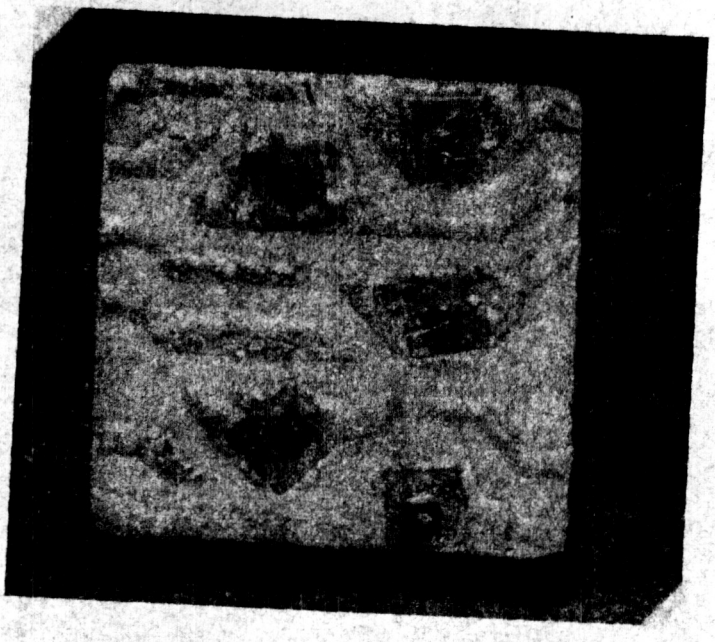


Figure 2-24. Wire-Lead Semiconductor Devices as Previously Used in Fabricating ULD's

However, changes were required in both the materials and processes previously used to fabricate ULDs.

The wire-lead ULD's as used on the MFM were processed as follows: (1) the Pt-Au conductors were screened and then fired at 960°C, (2) resistors were screened and then fired at 740°C, (3) the resistors were overcoated, (4) the top conductors were soldered with Indalloy 10 (75 percent Pb, 25 percent In), (5) the edge and bottom wrap-around conductors were soldered with Alpha 903 (62 percent Sn, 36 percent Pb, 2 percent Ag), (6) the resistors were trimmed, and (7) the wire-lead devices were attached and the ULD was encapsulated. The wire-lead devices were attached individually through localized reflow of the Indalloy solder by a resistance heating technique. There was a great deal of variation in the solder joints; however, there was no problem with diffusion of the Pt-Au conductor layer due to processing.

The wire-lead process was modified for ULDs using leadless semiconductor devices, since furnace reflow of 10/90 Sn-Pb solder is required to connect the terminals on the bottom of these devices to the ULD: First, the substrate conductors are dip-coated with 10/90 solder. All leadless devices required to complete the ULD circuit are then properly positioned over their respective conductors and connected simultaneously during the furnace reflow operation. The changes in the ULD conductor, solder, insulating, and encapsulating materials required to accommodate the 10/90 solder and the furnace reflow technique are subsequently described.

(4) Conductors and Solder

Because of the smaller size and increased accuracy of the conductor electrodes required by leadless devices, improvements had to be made on the artwork, photo-processing, and screen printing of the conductors: The grid system and film-stencil technique of forming conductor patterns provided the necessary accuracy in the original artwork. Additional control of the photo-processing steps provided the accuracy required for the final glass master. Accuracy in the screening process was obtained by employing a 325-wire-per-inch mesh for the screen stencils in place of the 200-wire-per-inch mesh used previously.

Also inherent with using leadless conductor electrodes on ULD's was the potential problem of an arc or corona discharge occurring under vacuum conditions. This could occur because of the small, 0.005-inch nominal lead separation. To determine the seriousness of this problem, sample ULD's using leadless electrode patterns were subjected to high voltages at reduced atmospheric pressures. Approximately 900 volts were required to initiate a breakdown at atmospheric pressure, and a minimum of 375 volts was needed to initiate a breakdown under the worse-case condition of pressure and electrode spacing.

The results of these voltage/pressure tests agreed with a theoretical analysis made on the breakdown phenomenon. The conclusion of this investigation, therefore, was that for the voltages present in the Saturn V computer an electrical discharge cannot occur between the electrode patterns used for leadless-device attachment.

The following investigations by Materials Engineering were made on the Pt-Au conductor paste.

- Conductors were screened with from one to five thicknesses of paste and tested for tensile bond strength. The strength improved rapidly up to a thickness of 0.00045 inch and leveled off to a gradual increase with thicknesses up to 0.00250 inch. A drawing and a photograph of the Pt-Au tensile bond strength fixture used for this and other tests on conductor adhesion are shown in Figures 2-25 and 2-26.

- A quantity of fully fired conductors were overscreened and refired. The tensile bond strength improved.

- Specimens were screened and fired at three different temperatures: 760°C, 800°C, and 960°C. The tensile bond strength increased with increasing temperature up to 960°C. Conductor diffusion into the solder was greater when lower sintering temperatures were used.

- Storing the substrates for times up to 1 week before firing had no adverse effect on the conductor patterns.

- The conductor pattern adhered to the solder on a MIB from which a ULD (MFM type) was removed.

- Photographs of typical acceptable and rejectable conductor patterns were furnished to Quality Engineering for inclusion in the general inspection procedure for ULD's.

- An acid-resistant conductor paste recently developed by DuPont has been ordered for study. DuPont claims that this paste, No. 8036, can be plated without adversely affecting its bond strength.

(5) Resistors

The range of resistor values required for the ULD-packaged simplex circuits was accommodated by three basic resistor pastes of 500-ohm, 3.5k, and 10k per square mil resistivities. Four additional resistivities were obtained by mixing the three basic pastes. Simplex resistor pastes are described in IBM Specification No. 6009325.

Tentative viscosity limits were established, as was a procedure for continually testing both resistor and conductor paste viscosities. However,

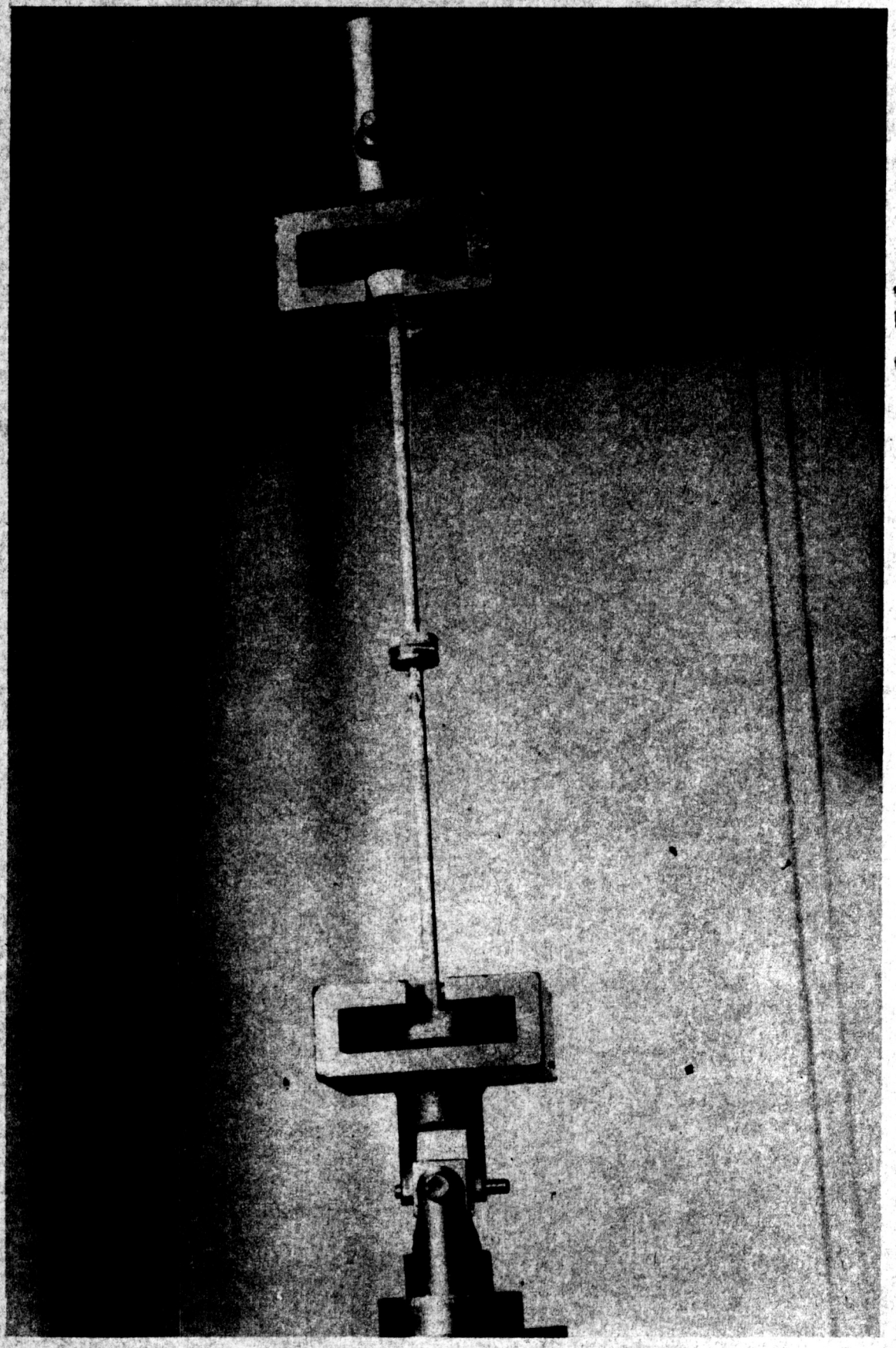


Figure 2-25. ULD Conductor Adhesion Test

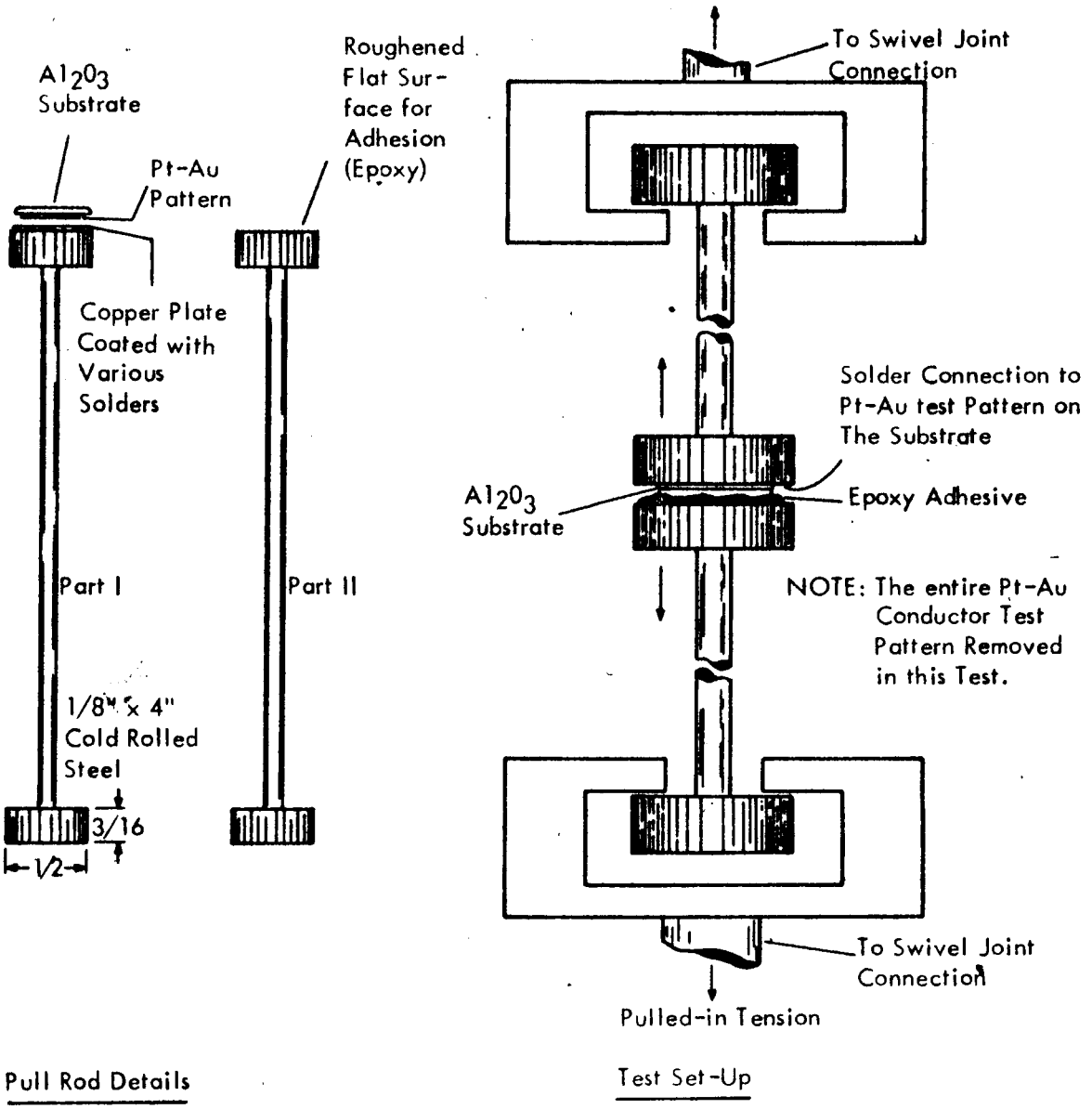


Figure 2-26. Pt-Au Tensile Bond Strength Test Fixture

additional control over screen process variables, such as temperature, squeege speed, etc., will be required before the full significance of viscosity control may be realized. An effort aimed at testing the basic resistor pastes for (1) TCR, (2) drift under load-life conditions, and (3) temperature stressing, is described in the Reliability section of this report.

One additional effort concerned the improvement of resistor trimming accuracy and efficiency through use of an improved trimming machine. This machine employs 20:1 templates for guiding the trimming nozzle of the air-driven abrasive unit, as well as a more accurate and convenient resistor monitoring scheme. ULD inverter module resistors, shown in Figure 2-27, before and after trimming with this apparatus.

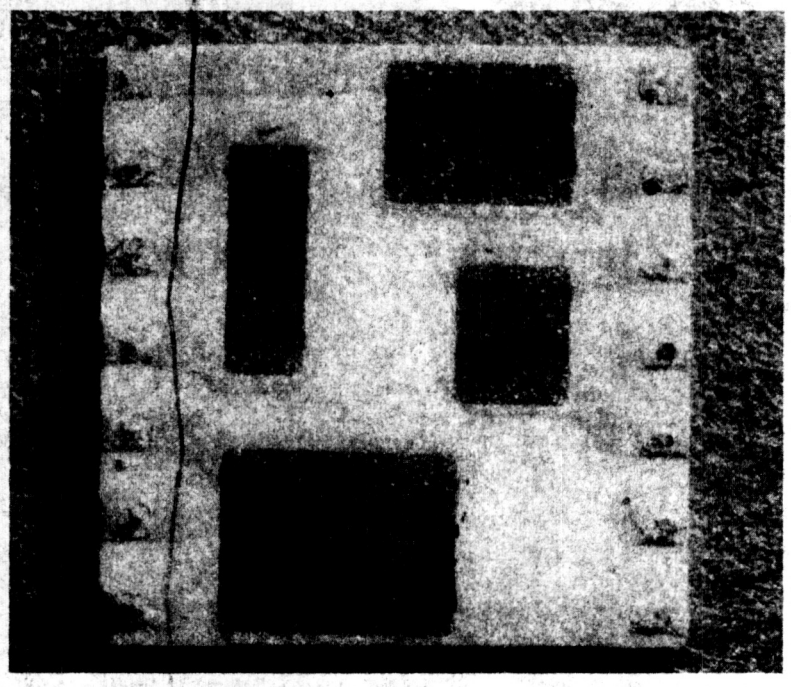
(6) Encapsulation

ULD's for the simplex computer will be encapsulated with RTV-60. While other materials are less affected by thermal environments and possess greater solvent resistance, the long-term effects of these materials on leadless semiconductors are not known. This fact, plus the IBM Components Division's experience with RTV-60 as an encapsulant for leadless devices, lead to the choice of RTV-60.

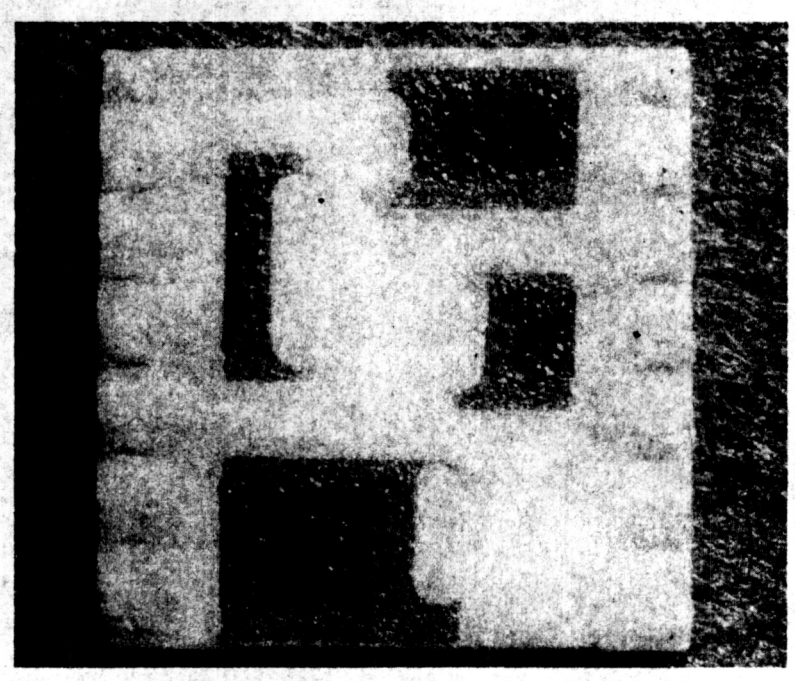
However, for ULD's intended for prototype computer use, IBM is developing an encapsulant which will meet the environmental and reliability requirements for later computers. One encapsulation technique developed by Materials Engineering has shown excellent results on initial samples; this technique is transfer molding of a glass-filled epoxy. Temperature cycling tests are being conducted on ULD's encapsulated by this method. The properties of other encapsulating materials and techniques are being studied and optimized to assure that the environmental requirements of prototype ULD's will be met.

(7) Insulating Materials

The change from lead-wire to leadless devices affected the insulating material used on the resistor side of the ULD. Previously, a material was applied to the bottom portion of the ULD to provide insulation between the ULD resistors and the MIB conductors, and to act as a solder stop on the bottom attaching area of the wrap-around conductors. However, because of the higher solder pot temperature (625°C to 640°C) required to apply the 10/90 solder, no material could be found to serve as both a resistor overcoat and a solder stop.



a. Untrimmed Inverter Resistors



b. Trimmed Inverter Resistors

Figure 2-27. Trimmed and Untrimmed Resistors on Bottom Side of ULD

As a substitute, Corning Glass powder 7052 mixed with a suitable screening oil, is screened onto the bottom of the ULD in two strips, as shown in Figure 2-28, following the resistor screening operation. The resistors and glass are then fired simultaneously. The resultant glass strips, in conjunction with a metal mask which holds the ULD during the dip-soldering operation, act as a solder stop to control the dimensions of the soldered areas on the bottom of the ULD. After the high-temperature soldering operation, an insulating coat (Laminar X-500-7-C-23) is applied on the bottom of the ULD between the glass strips. This insulating material has excellent moisture resistance and does not cause excessive resistor drift. A test has shown that this material does not lose its moisture resistant properties when subjected to the leadless-device joining temperatures.

(8) Hermetic Sealing

A back-up effort was conducted to develop a hermetically sealed package to relieve the plastic encapsulant from providing environmental protection. The method developed involves sealing a ceramic preform "square doughnut" to the substrate, followed by application of a flat metal top cap.

Samples of the ceramic preform spacer were purchased and a reproducible glass seal was made between the spacer and a substrate. This seal is accomplished by first screening and prefiring a glass-oil paste on the bottom of the ceramic spacer, and then placing the spacer on a substrate and firing it in a continuous conveyor-belt oven. By this technology the seven conductor patterns on either side of the substrate function as vacuum feed-throughs in the glass seal. Under leak tests this glass seal showed no leaks down to the accuracy of the testing apparatus (10^{-10} std cc of He per sec).

The flat upper surface of the spacer is metallized by screening and firing a metallic paste prior to obtaining the glass seal. After the glass seal has been made, the surface of the substrate and the upper surface of the spacer are tinned with solder. Active components are then mounted on the substrate inside the spacer. A Kovar top cap is then prepared with a small hole punched in its center, and solder is applied around its edges. The solder seal between the module and the top cap is obtained in an oven by solder reflow. After removal from the oven, the hole in the top cap (which permitted "breathing" of the module during sealing) is hand-sealed with solder. The wrap-around edges are then tinned with solder, resistors are trimmed, and the module is mounted on a printed circuit board.

Complete active samples are presently being constructed to demonstrate the reliability feasibility of this packaging technology.

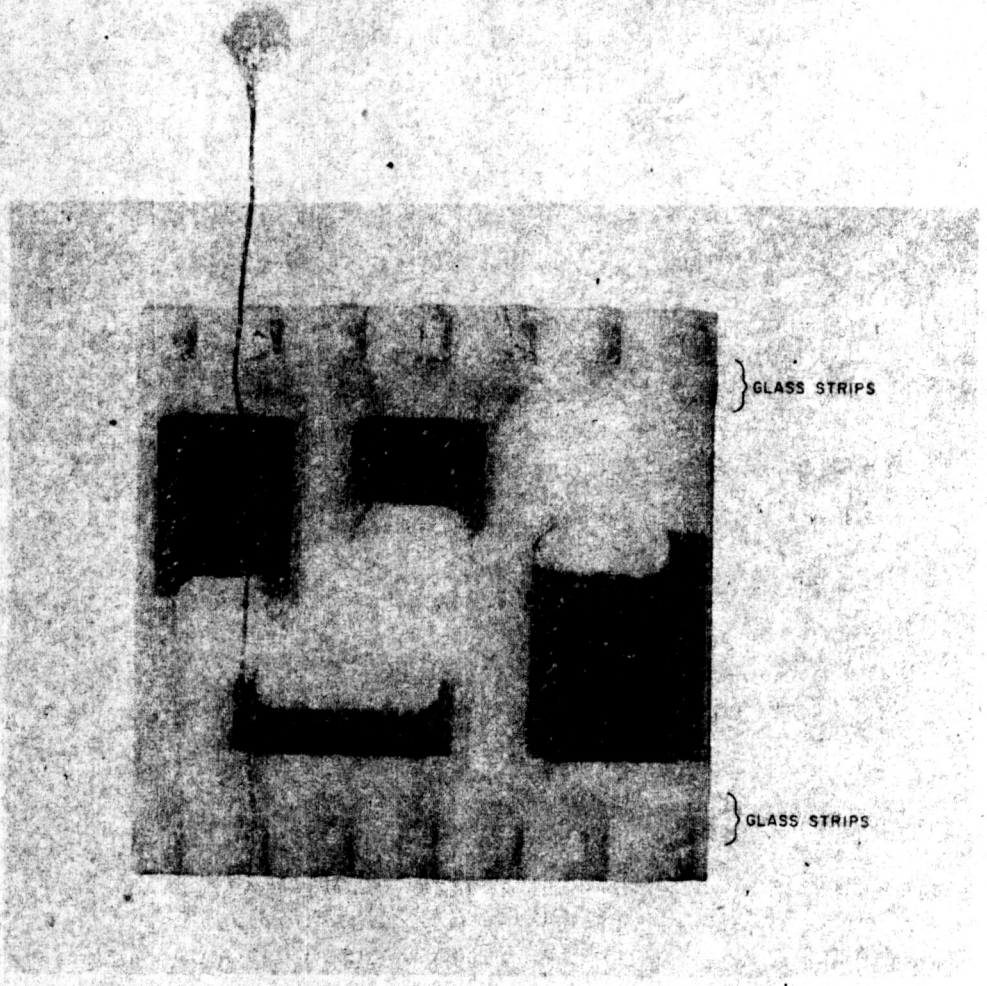


Figure 2-28. Glass Strips Used to Control Solder Dimensions on Bottom Side of ULD

f. Multilayer Interconnection Boards (MIB's)

MIB's on the logic pages contain 12 layers of copper for signal and power connections, as illustrated in Figure 2-29. Front and rear views of a test MIB are shown in Figure 2-30, and the top land pattern, a typical signal layer, and a ground layer are shown in Figures 2-31, 2-32, and 2-33, respectively. Each MIB measures $3.00 \times 2.62 \times 0.06$ inches.

Of the 40 MIB types required for the breadboard, 30 have been released for production. Artwork for the remainder has been generated and will be released soon. Page MIB's are being fabricated for environmental tests. Sample MIB's made in the form of a constant stress beam (Figure 2-34) are being used to determine static and fatigue strength characteristics of the boards, plated holes, and circuits. The fatigue test installation is shown in Figure 2-35.

g. Back Panels

Pages in each computer channel are interconnected through a back panel MIB that contains 14 layers of wiring. Connector receptacles for the pluggable pages are soldered into plated holes in the back panel. A metal plate is used to stiffen the assembly to withstand the connector engagement force.

The breadboard computer back panels are wider than necessary to permit greater spacing between page connectors. In addition, all etched circuit lines to the connector terminals are placed on the outer surface of the board. These two features have been included to facilitate back panel rework for circuit modifications. The three logic back panel MIB's have been designed, and artwork is being generated.

h. Flat Cables

Back panels are interconnected by etched flat cables and terminal blocks, as shown in Figures 2-36 and 2-37. The terminal blocks contain pins which are soldered on one end into plated holes in the back panels, and soldered on the other end to the flat cable conductors. The blocks support both ends of the cables. The center section of each cable joining the back panels is flexible.

The cables are etched from a two-sided, copper-clad, Fiberglas teflon laminate. Signal wiring is etched on one side, the ground or power plane is etched on the other. Teflon insulating layers are applied over the exposed copper surfaces except in soldered areas. Front and rear views of an experimental cable are shown in Figure 2-38.

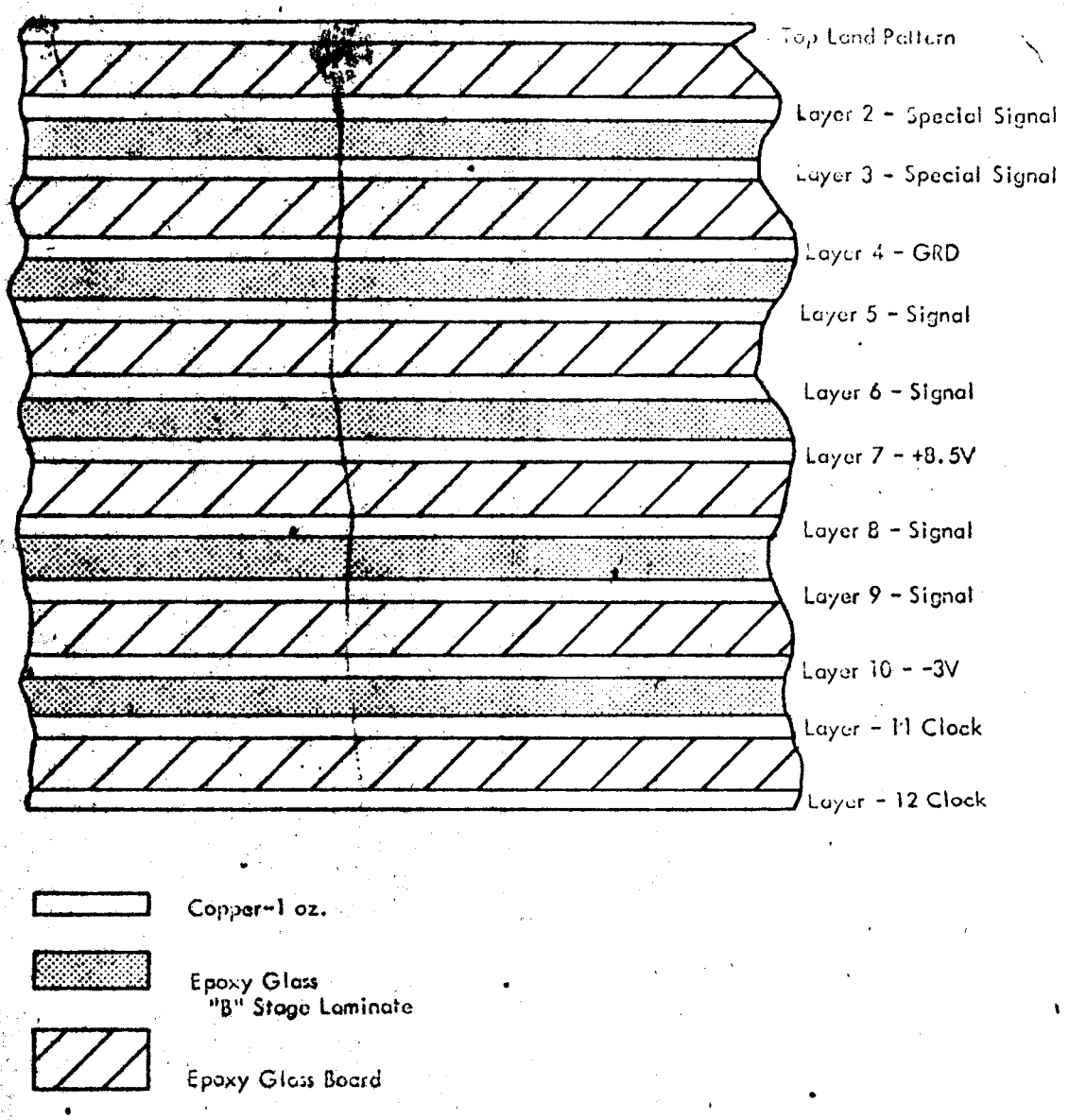


Figure 2-29. MIB Layers

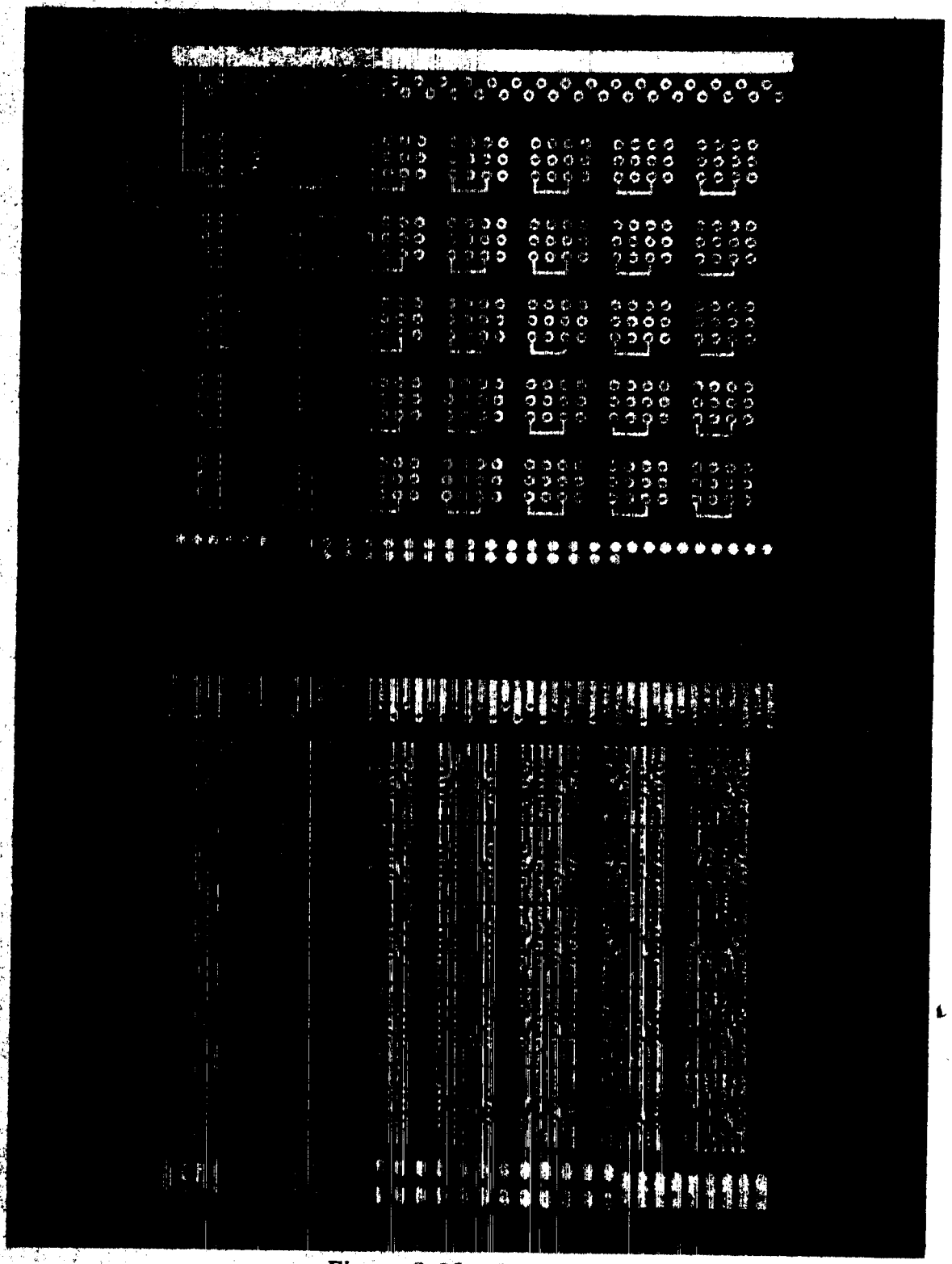


Figure 2-30. Page MIB

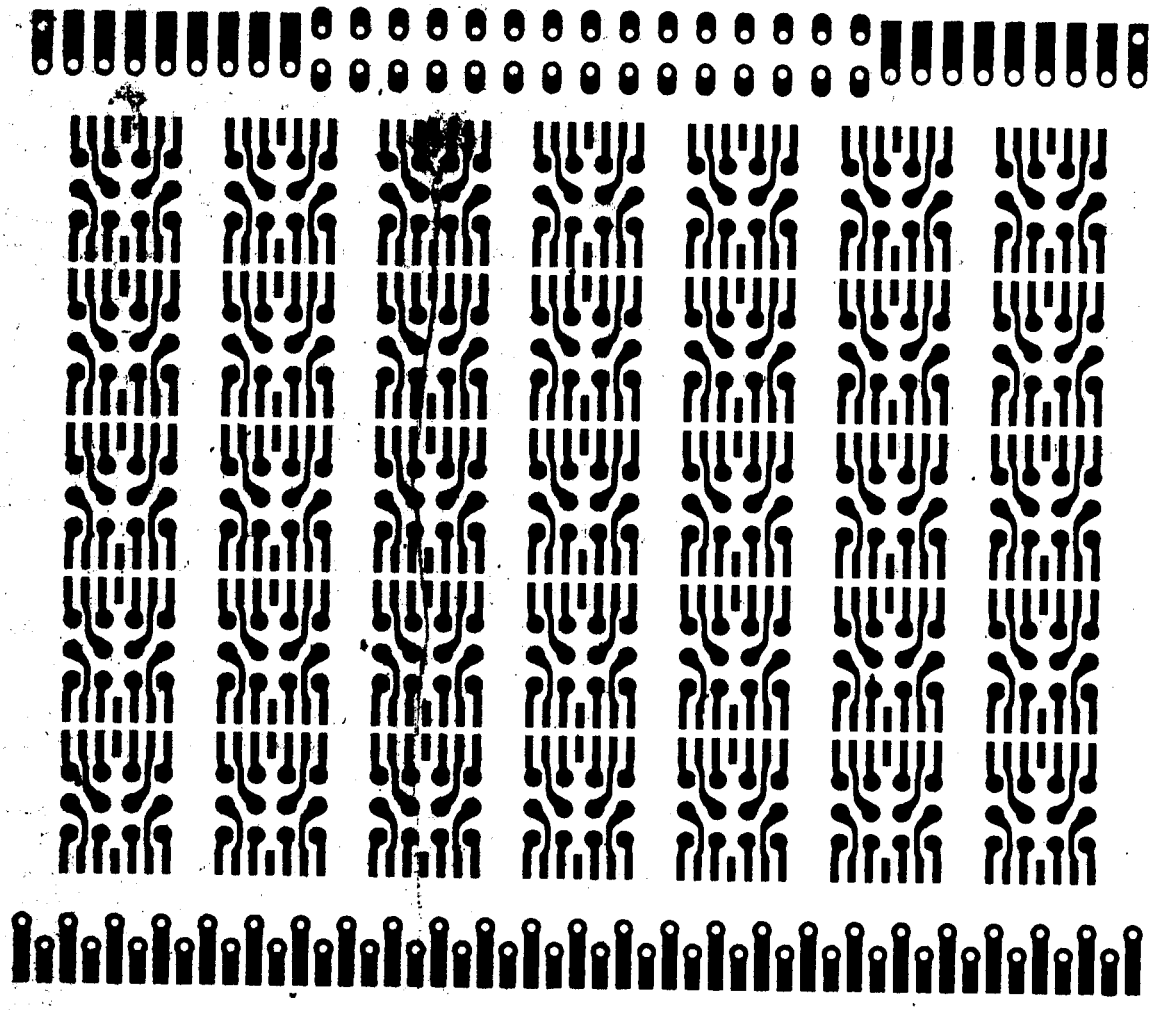


Figure 2-31. Page MIB Top Land Pattern

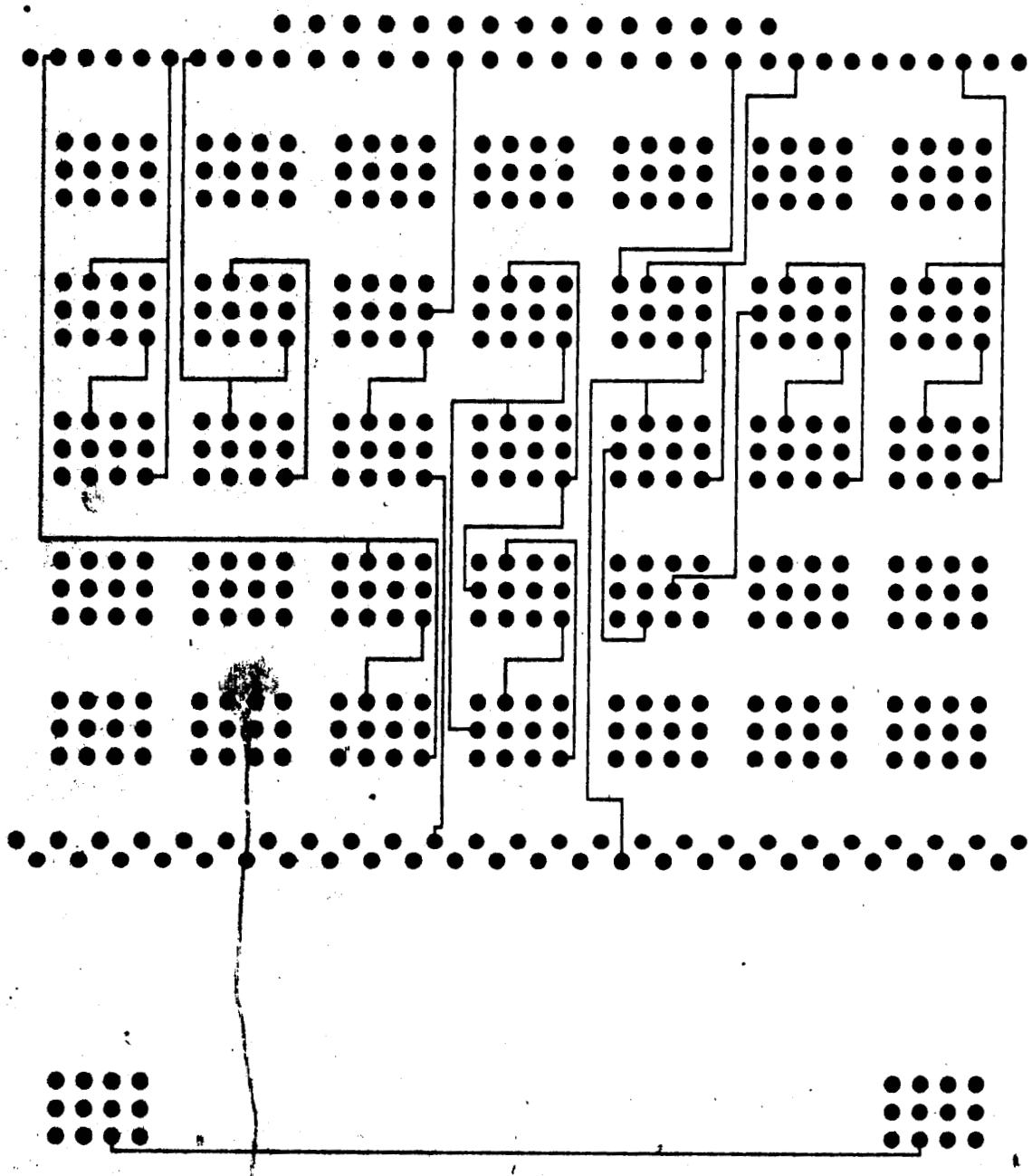


Figure 2-32. Page MIB Signal Layer

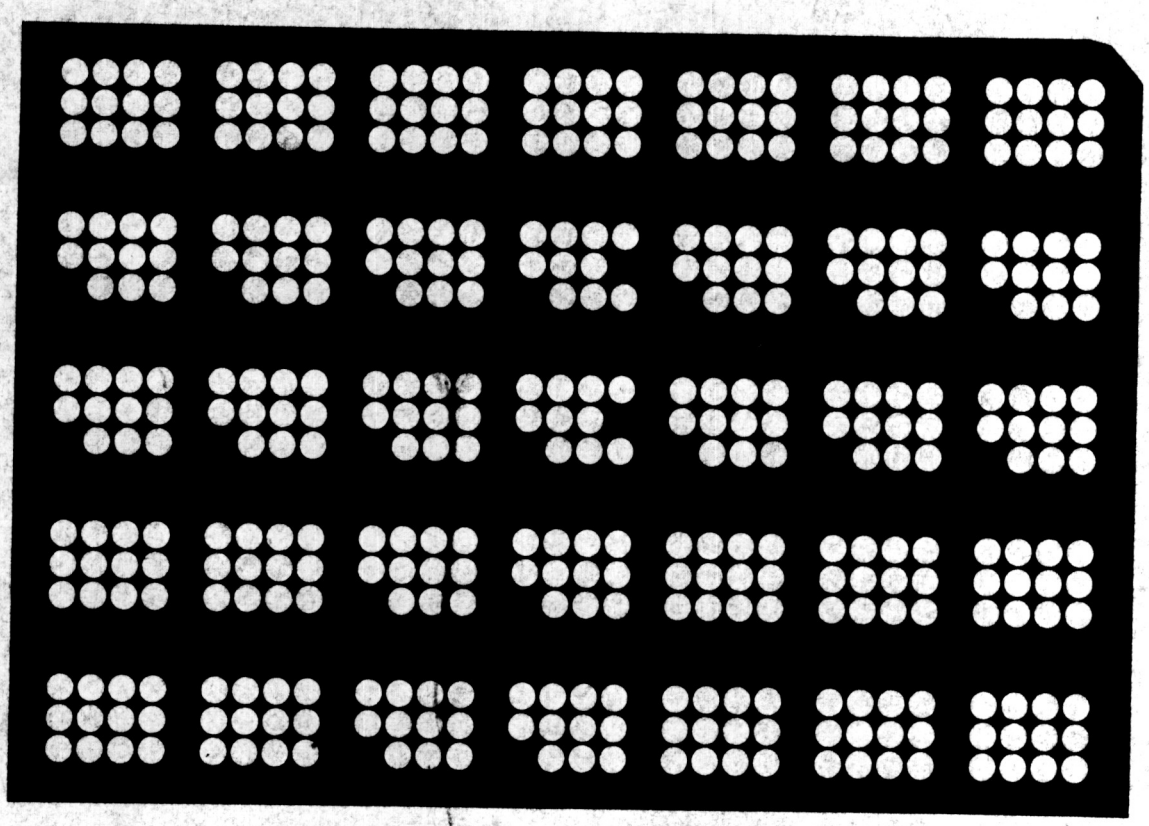


Figure 2-33. Page MIB Ground Plane

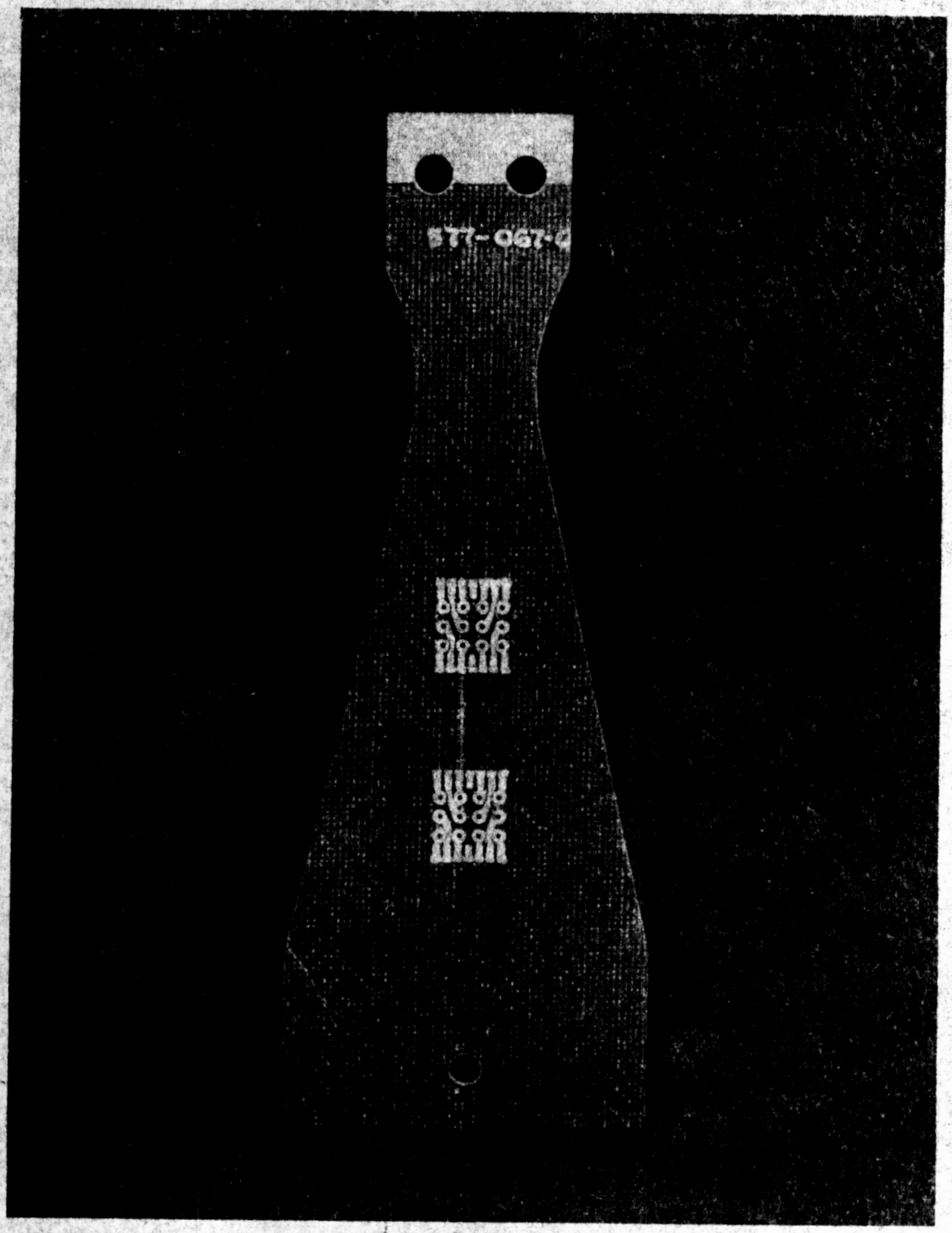


Figure 2-34. Constant Stress Beam MIB

Figure 2-35. MIB Fatigue Test Installation

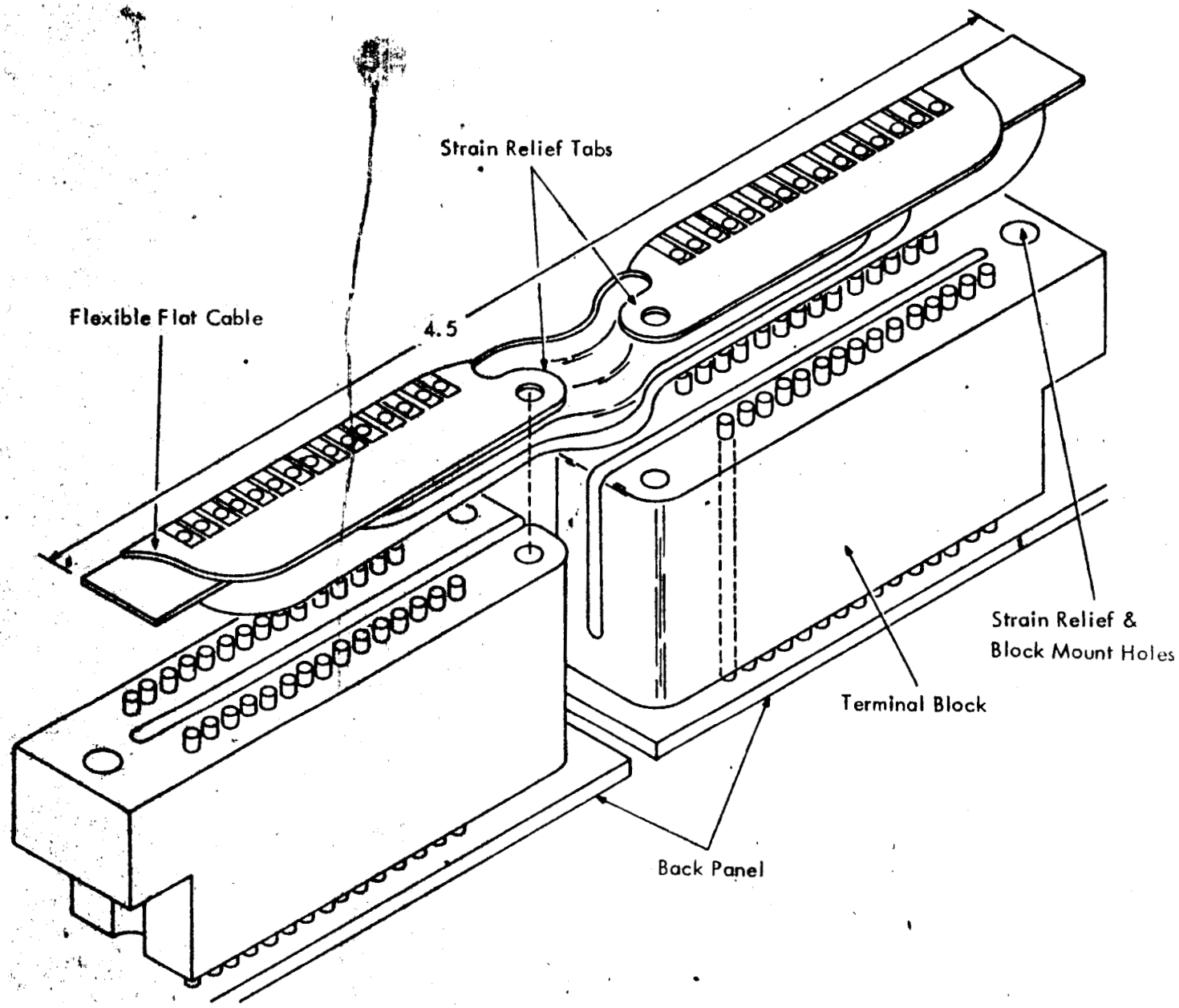


*Figure 2-36. **Breadboard** Back Panel Interconnection Flat Cable*

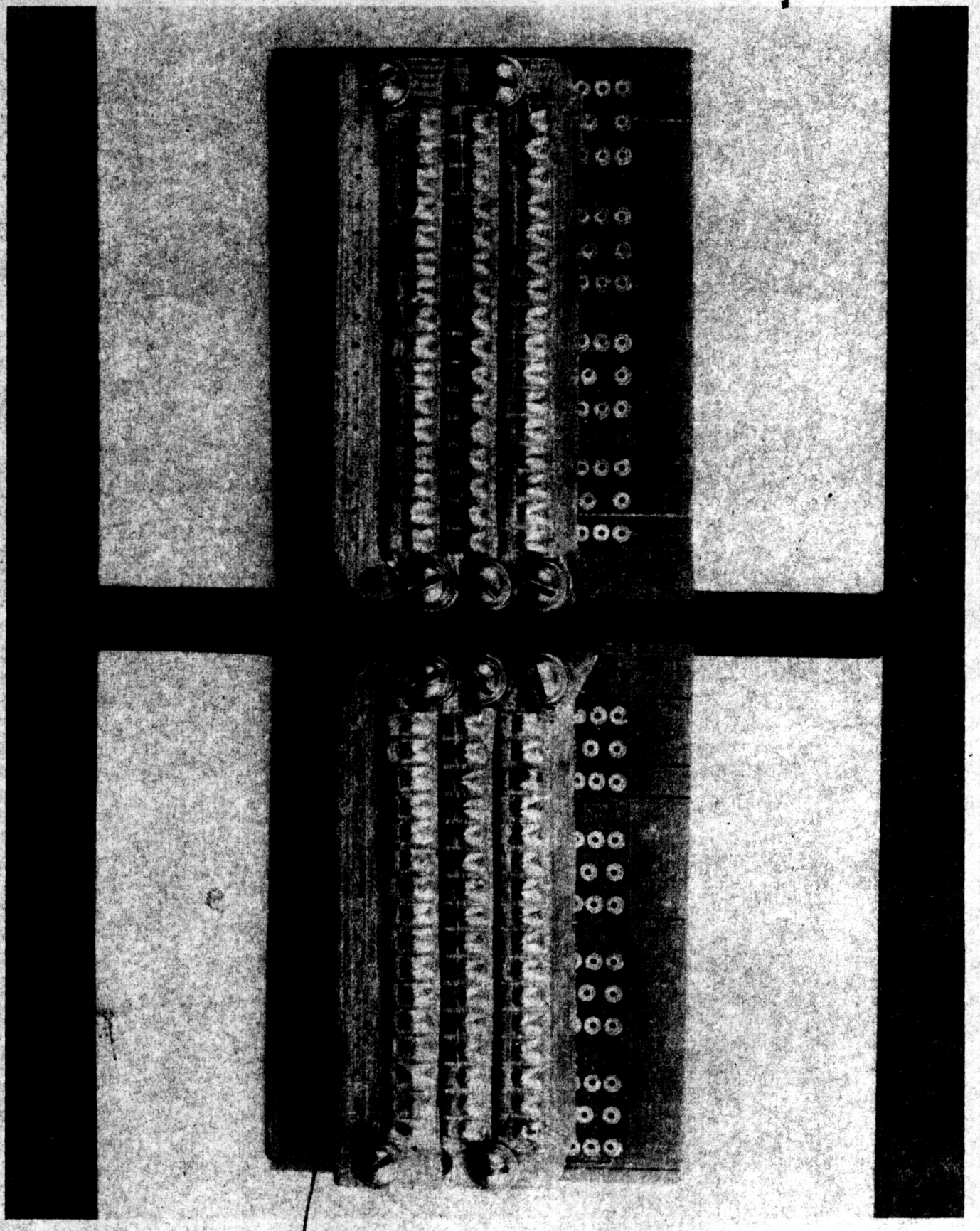


Figure 2-37. Breadboard Back Panel Interconnection Cables and Terminal Blocks

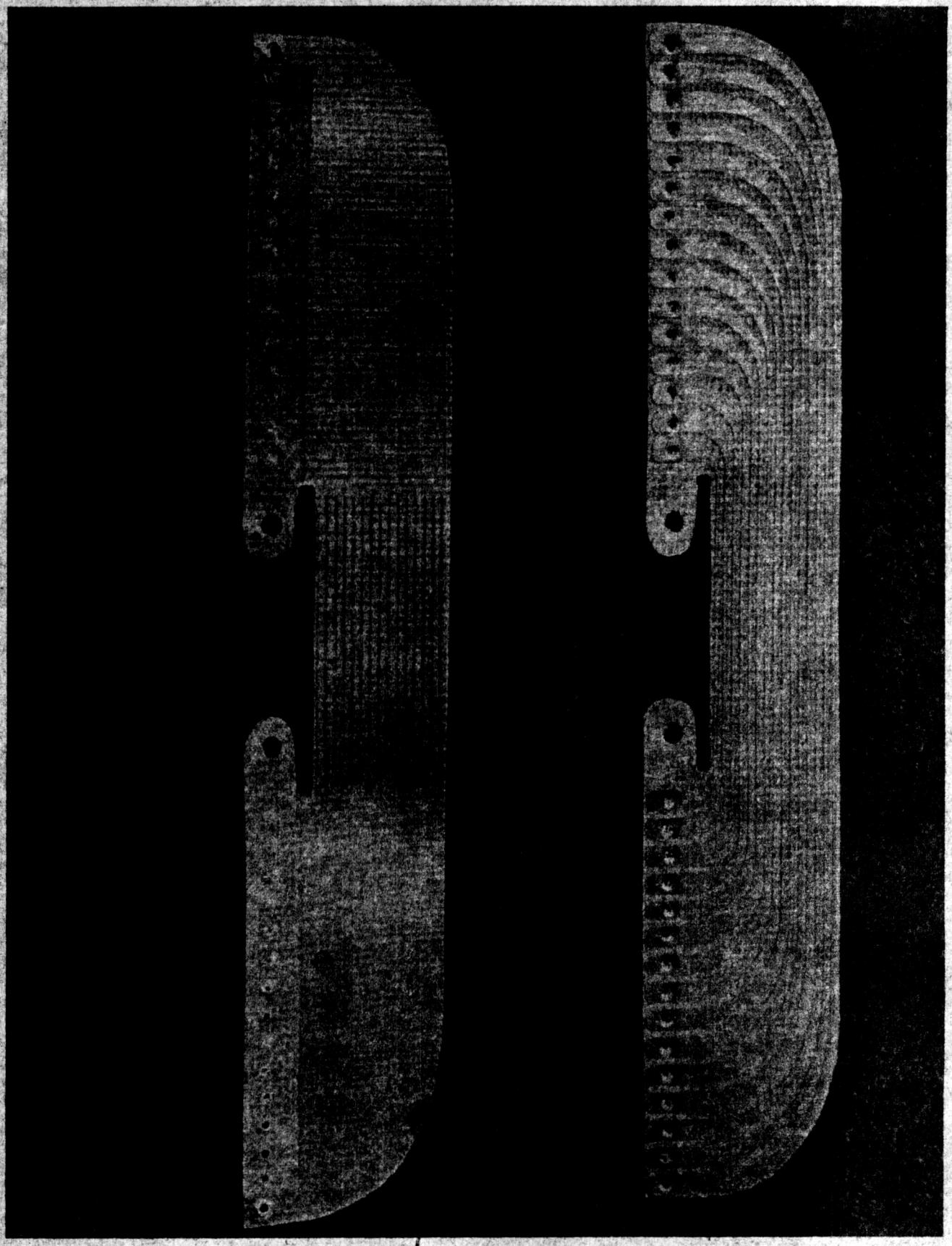


Figure 2-38. Flat Cable

Similar flat cables connect the back panels to the Bendix pygmy external connectors on the computer. An adapter block is fastened to the connector to make the transition between connector and cable (Figure 2-39).

The cable to the memory requires greater flexibility than the others because it is terminated in a pluggable connector that may be disconnected to remove the memory. The highly flexible portion of the cable has all conductors in one plane. Shielding is accomplished by alternating signal and ground conductors.

All eight cable types used in the logic section have been released for production. The cables required to connect the logic and memory are being designed.

2. TMR COMPUTER

a. General

Interconnections for the TMR computer are similar to those for the breadboard computer but differ in the ways described below. The TMR logic section contains five channels, with the first three identical. Channels 1, 2, and 3 each contain 18 pages, while channels 4 and 5 contain 10 and 12 pages, respectively. The general layout of the TMR computer is shown in Figure 2-40.

b. Page and Support Mechanism

TMR computer page size, materials, MIB construction,and connectors are identical to those used in the breadboard computer. However, thermal tests on the page support mechanism showed that an improved heat transfer path is required between the page and computer structure for proper operation in a vacuum. To solve this problem, pages and heat-path clips with several combinations of surface treatments were tested in a vacuum to determine temperature difference between page frame and computer structure. In addition to the page and spring clip combinations, an experimental page with a wire-mesh heat path was tested. Although the "wire-mesh" page would require modification for use in the computer, its excellent heat transfer characteristics indicate that an improved page support mechanism design can be found. The results of these thermal tests, conducted for initial page insertion at 8 watts dissipation, are presented in Table 2-VI.

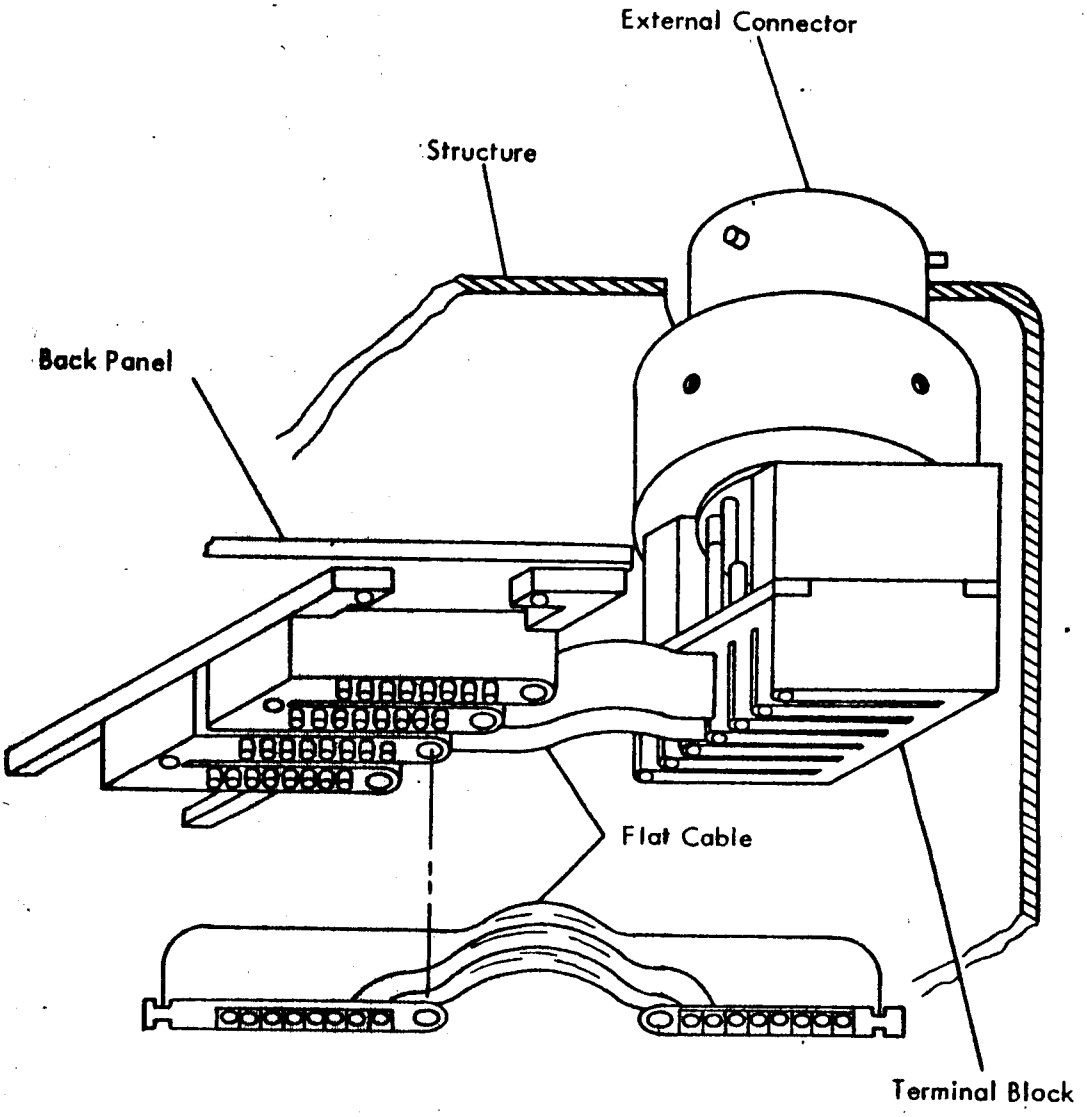


Figure 2-39. Flat Cables to External Connector

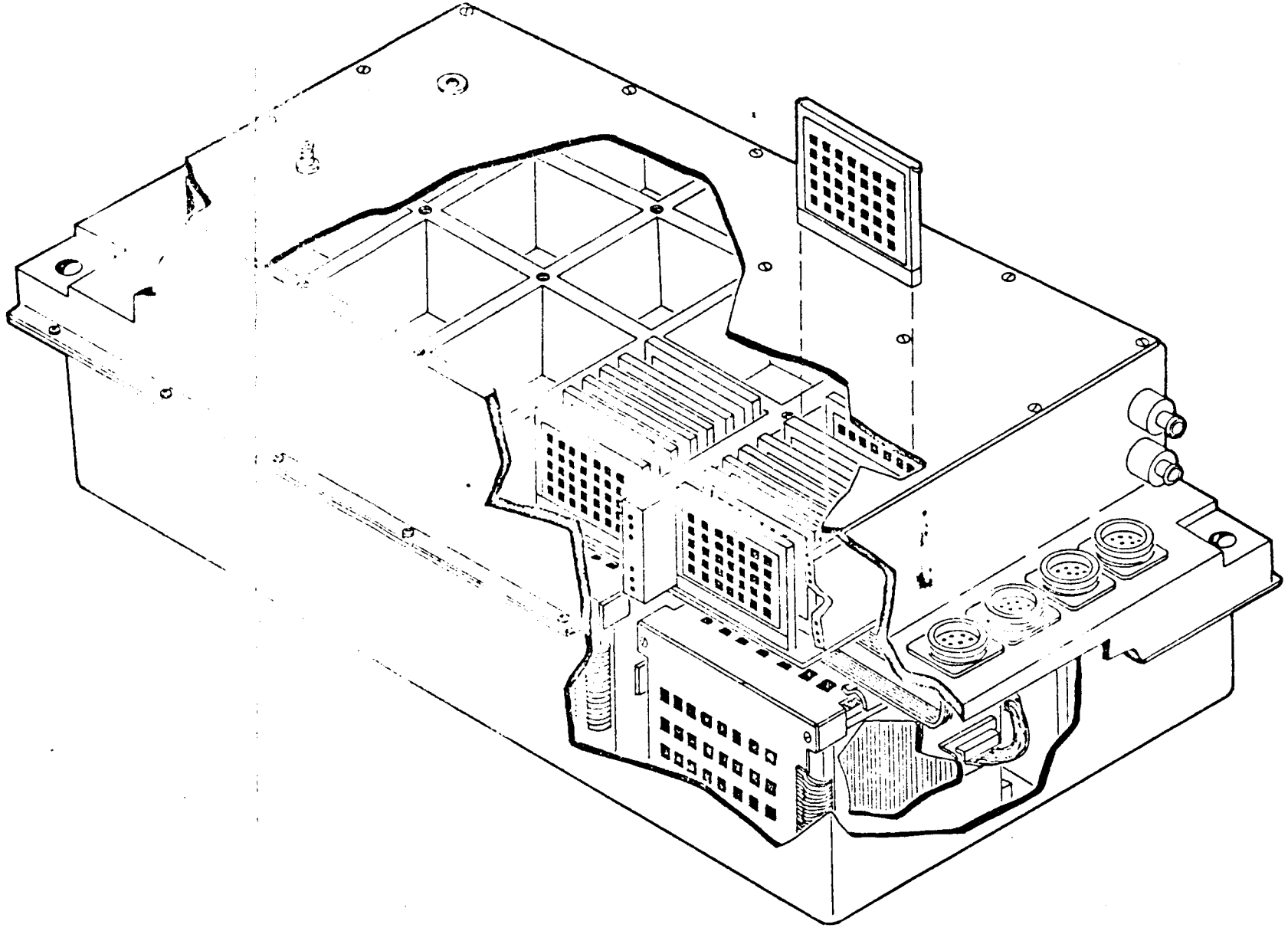


Figure 2-40. TMR Computer General Layout

Table 2-VI

Thermal Test Results

Page No.	Page Material	Page Surface Treatment	Clip Material	Clip Surface Treatment	Average Page-To-Structure ΔT (°F per (watt)
1	Magnesium-Lithium	Polyurethane	Beryllium Copper	Tin	5.4
2	Magnesium-Lithium	Nickel	Beryllium Copper	Nickel	5.3
3	Magnesium-Lithium	Tin-lead	Beryllium Copper	Tin	6.6
4	Magnesium-Lithium	Polyurethane	Beryllium Copper	Chromium	7.8
5	Magnesium-Lithium	Epoxy	Beryllium Copper	Tin	11.1
6	Magnesium	Tin-lead	Copper Mesh	None	2.5

c. Flat Cables

The flat cables and terminal blocks for the TMR computer were modified to reduce the volume required for (1) the cables which interconnect the back panels, and (2) the cables which connect the back panels to external connectors. For connections between back panels, each pair of terminal blocks will support 12 cables of 12 conductors each, as shown in Figure 2-41. A similar arrangement will be used to connect back panels to external connectors and to the memory junction board. Preliminary design work has been completed for some cables and terminal blocks, and evaluation samples are being fabricated. Back panel layouts are being studied to determine connection densities in the cable termination areas.

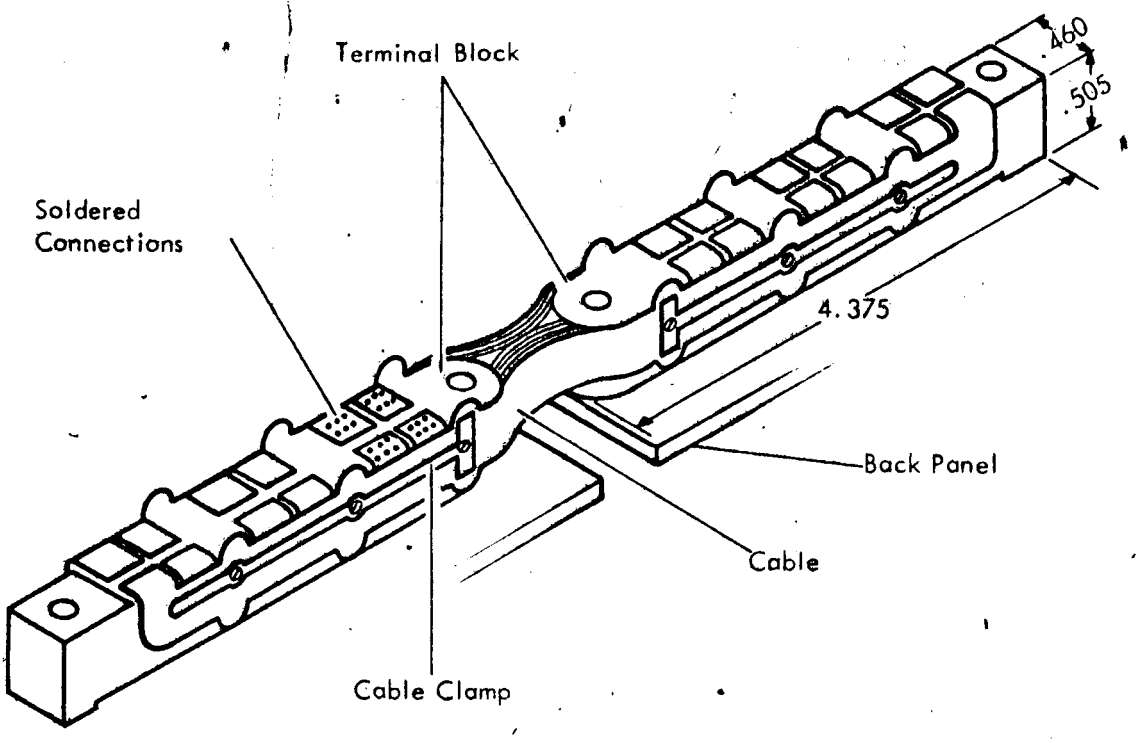


Figure 2-41. Back Panel Interconnection Cables

D. SIMPLEX COMPUTER MECHANICAL DESIGN

The structural design of the simplex computer is complete. The design drawings have been released to the model shop, and fabrication of the parts is 70 percent complete. The final design should be completed by 30 October.

E. TMR COMPUTER MECHANICAL DESIGN

1. STRUCTURE: DIMENSIONS, VOLUME, AND WEIGHT

The present TMR computer, when it employs six memory modules (Figure 2-42) is 12.8 × 32 × 10.5 inches in size, occupies 4095 cubic inches of swept volume, and weighs 88.7 pounds. The respective figures for a computer which employs eight memories are 12.8 × 32 × 12.5 inches, 4875 cubic inches of swept volume, and 95.0 pounds. These specifications are subject to change, due to the advances being made in logic design.

The following manufacturing techniques are being considered for the computer structure:

- Machine the structure from a solid billet and then rifle bore liquid flow paths within the walls.
- Machine the structure from a solid billet which contains preformed stainless-steel tubing for carrying liquid coolant.
- Fabricate a casting and finish by machine. This casting shall contain either rifle-bored cooling paths or cast-in stainless-steel tubing.

2. MEMORY CONFIGURATION

a. Requirements

The present computer is designed to house six or eight memory modules, each 6.250 × 4.865 × 5.528 inches (Figure 2-43). Regardless of whether six or eight modules are used, they will be bolted to the underside of the interior structural framework with the 6.250-inch side located in the X axis of the computer (see Figures 2-42 and 2-43).

b. Memory Module Design

The original memory module design employed the standard RANDAM core plane (64 × 64 T-39 MARS device matrix) in a 28-plane array. This design effort primarily involved packaging the associated electronics in a

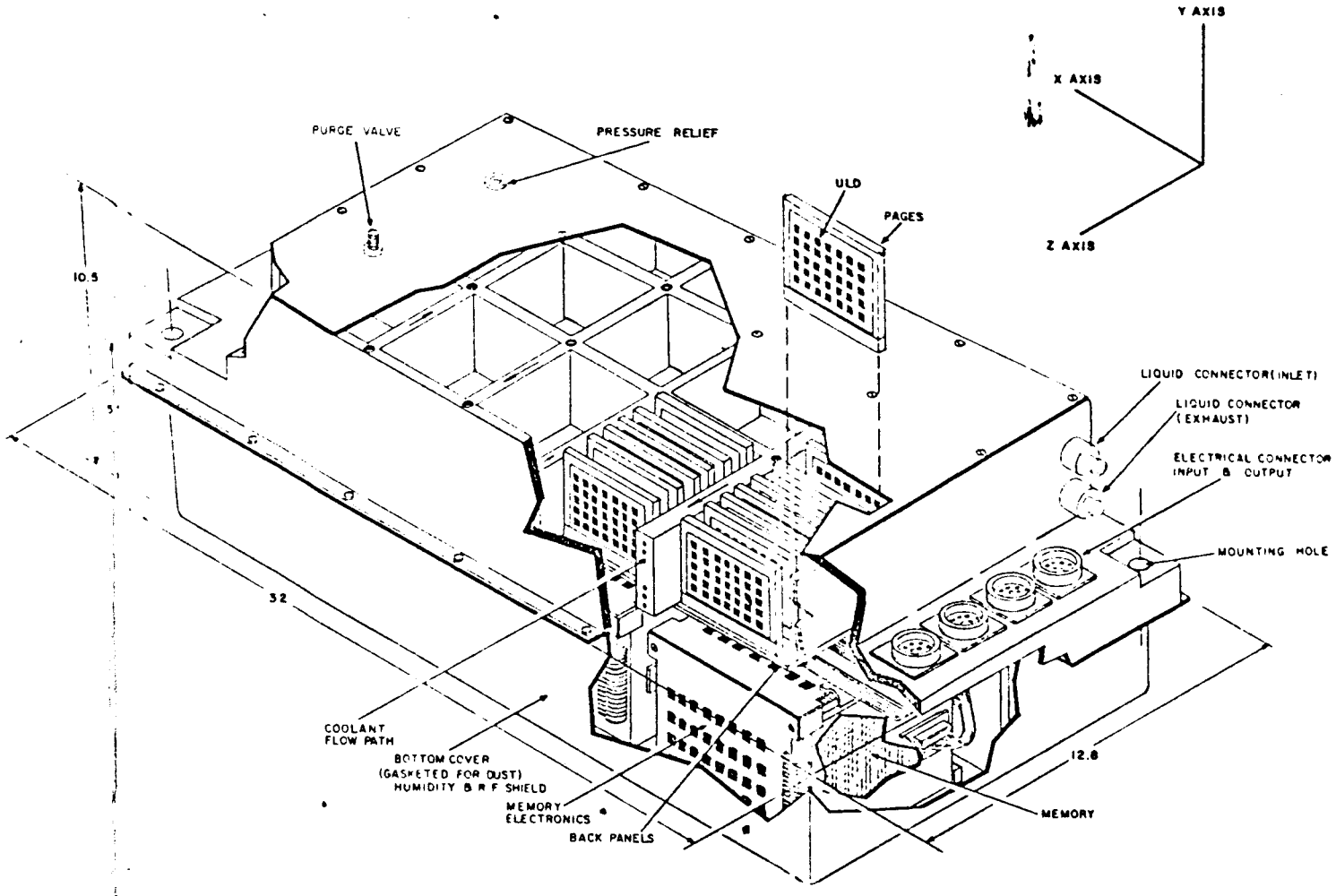


Figure 2-42. Saturn V Guidance Computer, General Design

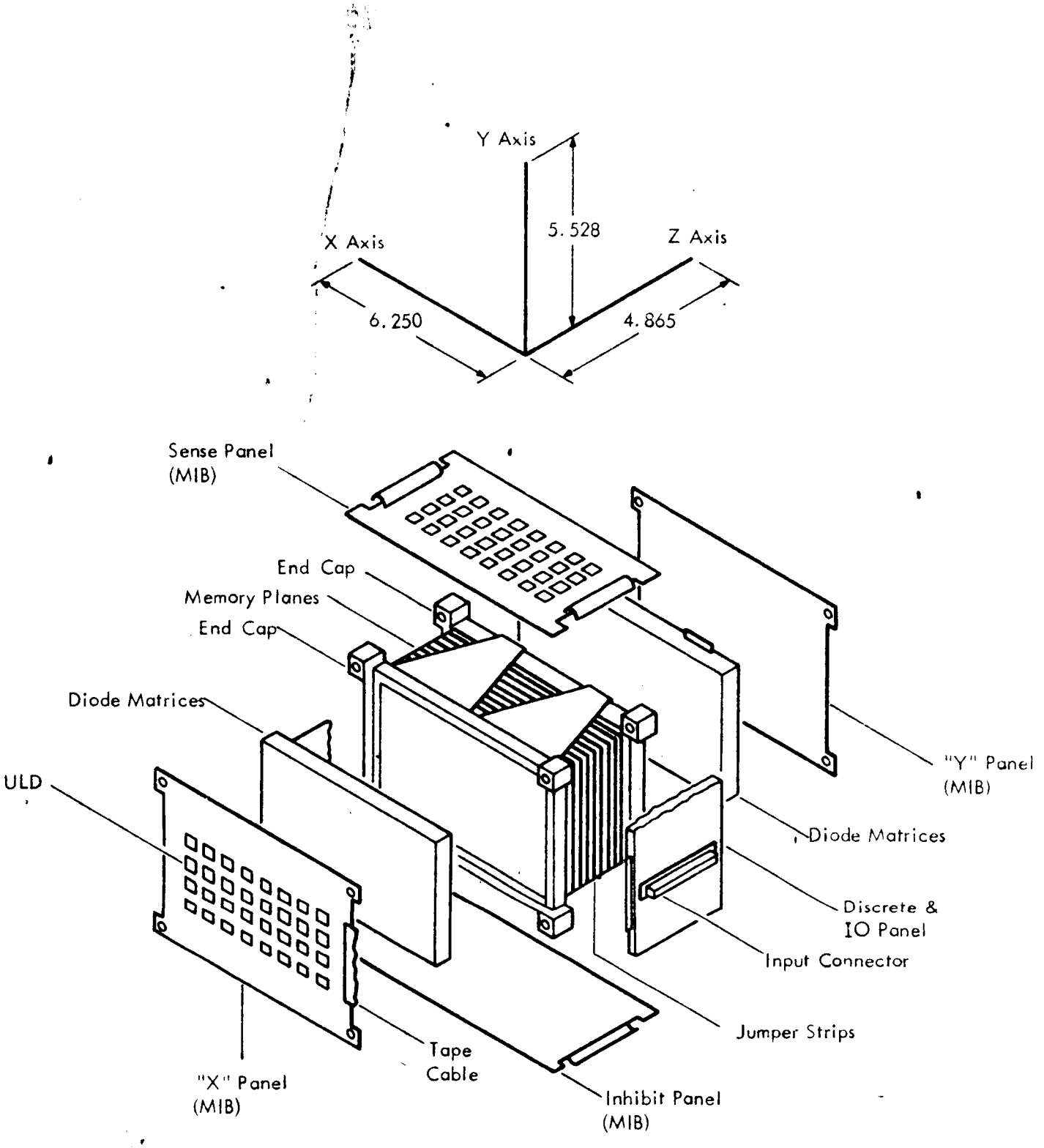


Figure 2-43. Memory Module Design

manner to meet thermal and vibration environments. The electronics were to be mounted directly on the array.

The memory module design was in the study stage when the directive to replace the T-39 MARS devices with T-38 toroids necessitated a redesign of the array and associated electronics. The preferred arrangement from an electrical drive viewpoint consisted of two 14-plane arrays per memory, each plane having a 64 × 64 toroid matrix. However, this presented an interconnection problem. This concept was retained while the plane-to-plane interconnection problem was substantially reduced by using a single 14-plane array per memory, each plane having a 64 × 128 toroid matrix. The associated memory electronics are attached to the array to form the memory module (Figure 2-43).

The initial design work on the plane frame resulted in a one-piece structure of Hysol MH 3-4896 with molded-in terminals. The array of 14 planes is interconnected on all four sides by printed circuit jumper strips and is held together by metal end caps at the four corners of each extreme. The caps are connected by four rods passing through corners of the array. All the electronic subassemblies are mounted to the array at the end caps, and mounting lugs on the caps are used to attach the memory module to the computer structure. The structure of the electronic subassemblies adds to the rigidity of the memory array, allowing the memory module to be mounted on the computer structure at only two points on each end cap. The memory's metallic structure conducts heat from the electronics to the end caps; it is ultimately dissipated to the coolant passages within the computer structure.

The memory X-panel consists of a metal sheet sandwiched between two MIB's; the outside surface of each MIB serves to mount electrical components. Spacers separate the X-panel from the X-diode matrix.

The Y-panel is similar to the X-panel except that one MIB is bonded to the metal plate. The Y-panel is attached to the Y-diode matrix.

On the mounting-lug side of the memory is an assembly that includes the TVC and timing subassembly on one side of a metal plate and the inhibit panel on the other side. A MIB and a double-sided printed circuit board with electrical components mounted between them form the TVC and timing assembly, while a MIB with components on the outer surface comprises the inhibit panel. These details are illustrated in Figure 2-43.

The electronic assemblies are interconnected by tape cables soldered to pins. Electrical entry and exit from each memory module is provided by one 98-pin connector (identical to that used on each logic page) mounted on the input/output panel.

c. Memory Design Status

The memory design has progressed as follows:

(1) Jumper strips (interconnecting planes) - released in September.

(2) Diode matrix design completed - all drawings released in September.

(3) Plane assembly drawing - completed and released in August.

(4) Sense and inhibit printed circuit panels - completed and released in September.

(5) X and Y MIB's (electrical packaging development effort) - completed and released in September.

(6) All panel support plates - completed and released in September.

(7) Tape cables, the distribution panel, and hardware are 50 percent complete.

(8) The TCV and timing subassembly was completed, except for the MIB layout, and released.

(9) The memory frame mold design was completed, and fabrication is 50 percent complete.

(10) The structure design part details are 75 percent complete, with remainder awaiting completion of electronic subassembly design to assure that proper heat transfer characteristics are included.

d. Vibration and Stress Analysis

The X-plate panel and inhibit panel were vibration tested, and their vibration characteristics and the stresses induced by the vibrations were analyzed. By using the equation for the vibration of a free plate and considering only the magnesium plate rigid, the following conservative natural frequencies were obtained: (1) inhibit panel, 632 cps; and (2) X-plate panel, 194 cps. At these frequencies and 30 G rms the centers of the X-plate panel and inhibit panel magnesium plates would have amplitudes of 0.011 and 0.0011 inch, respectively.

The stresses corresponding to these amplitudes, considering the plates as beams fixed across the short sides, would be as follows:

- Magnesium base of X-plate - 2750 psi.
- Magnesium plate of inhibit panel - 1160 psi.
- Epoxy glass boards of X-plate - 750 psi.
- Epoxy glass boards of inhibit panel - 83.5 psi.

The vibration characteristics of a memory array with foam-covered magnesium-lithium spacers were investigated by mathematical means. The natural frequency of such an array with planes encapsulated in Sylgard 182 would be slightly lower than the frequency of a system without spacers. Consequently, a foam spacer could be used for damping without a significant change in natural frequency.

The wire stress caused by the deflection of a memory plane was analyzed. If a wire across the center of the plane was deflected an amount y_o at its middle, the stress in the wire would be determined by the following equation:

$$S = \frac{E y_o \, 2\pi \, 2}{2L^2} ,$$

Where E is the modulus of elasticity, L is the length of the wire, and the following assumptions are used:

- No initial stress
- Stress is below the yield point.

For a plane 3.625 inches long and a wire with an E of about 17×10^6, a deflection of 0.075 inch would cause a stress of 36.9×10^3 psi.

e. Thermal Analysis

A thermal analysis was made on the inhibit driver panel. A first analysis using preliminary information indicated that a temperature differential of approximately 11°F existed across the inhibit panel. An inhibit driver ULD which used wire-lead devices was also analyzed, and an 11°F temperature differential was predicted. An estimated temperature differential of 40°F between junctions on this panel indicated that this design was unsatisfactory. The inhibit driver panel was then modified by using different components and packaging.

A thermal analysis of the memory unit indicated a temperature differential of 2°F through the memory core section. Temperature differentials of the various panels with reference to the mounting pads were as follows:

- Sense panel: 20°F
- X-driver panel: 34°F
- Y-driver panel: 34°F
- Inhibit panel: 46°F
- MCD panel: 8°F
- TCV panel: 19°F
- Diode matrix: 8°F

A more detailed analysis of temperature differentials within panels indicated the following differentials:

- X-driver panel: 2.5°F
- Y-driver panel: 1.3°F
- Sense panel: 2.6°F

The inhibit driver panel is undergoing a detailed thermal analysis. In this panel design the MCD and TCV panels are included in one block, which is mounted on the same plate as the inhibit driver panel.

The X-and Y-driver panels and the sense panel were analyzed by assuming that magnesium alloy mounting plates were used. The memory unit analysis was made assuming usage of aluminum parts.

Junction-to-junction temperature differentials across the panels will be predicted as the thermal data on these components become available.

f. Stress on the Ferrite Cores

The electrical characteristics of the toroid (T-38) and the MARS (T-39) memory cores were determined by subjecting the cores to tension, compression, and bending stresses. The most severe electrical degradations of the toroid cores were caused by stresses due to edge compression and tension (Figure 2-44). Compression and bending caused less severe degradation.

The most severe degradations of the MARS core were caused by bending stresses (Figure 2-45). Degradations caused by other stresses are also shown in Figure 2-45 and in Figure 2-46.

Stress test results on the memory cores lead to the following recommendations:

- The memory planes should be wired so that the wires do not put tension on the cores.
- The encapsulant material should have minimum cure shrinkage and temperature expansion characteristics and yet be rigid enough to enable the memory plane to withstand vibration.
- The use of a good damping material between memory planes would improve shock and vibration resistance.

g. Encapsulation Materials

The following eight encapsulants were tested on individual T-38 ferrite cores:

- Conap 1132, polyester
- Conap 57-59-1/52-59-1, epoxy
- Dupont Adeprene L-100, polyurethane
- GE SS-4090, SS-4093, silicone
- GE Sylgard 183, silicone
- GE SR-220
- Laminar X-500 (8C8/10C56), flexible polyurethane
- Laminar X-500 (7X1/10C32), polyurethane

Each material was used to encapsulate two cores, after which the electrical degradations of the cores were determined at room temperature (26°C). Those cores encapsulated in Conap 57-59-1, Dupont Adeprene L-100, and Laminar X-500 (7X1/10C32) showed complete degradation. The remaining cores have the following order of preferred usage based on this phase of testing: GE Sylgard 183, Conap 1132, GE SR-220, Laminar X-500, and GE SS-4090.

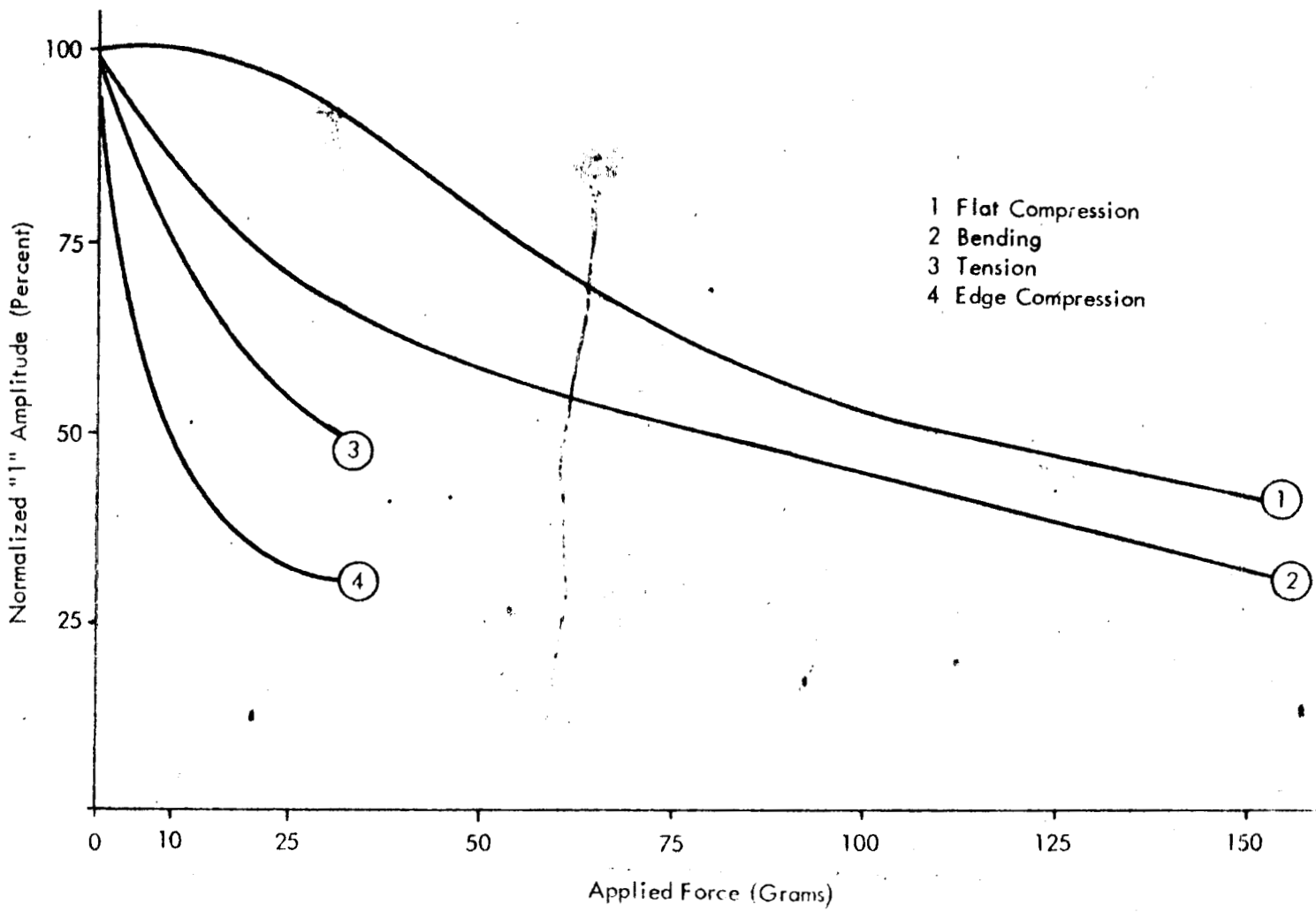


Figure 2-44. Results of Toroid (T-38) Memory Core Test

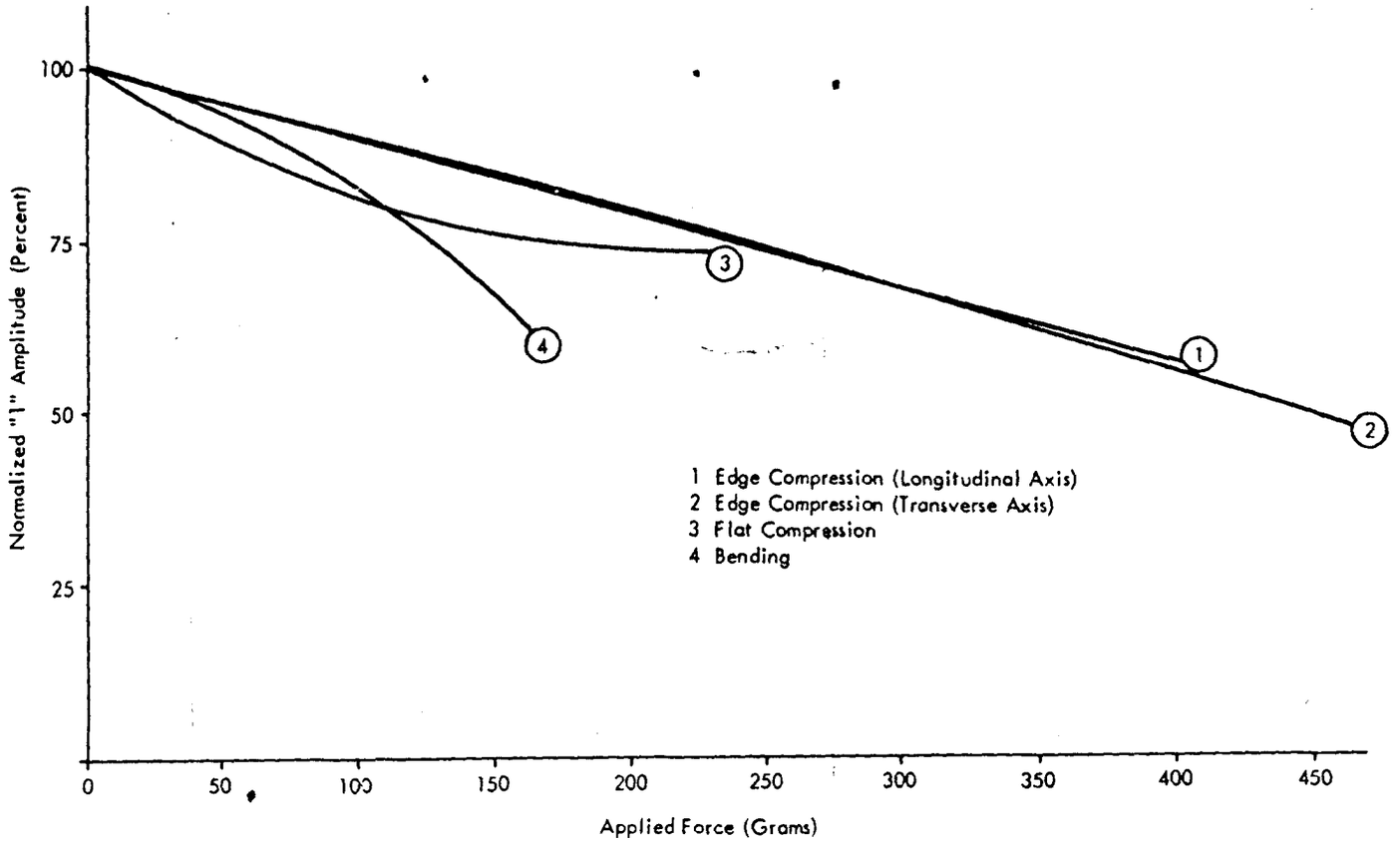


Figure 2-45. Results of MARS (T-39) Memory Core Test (Bending and Compression)

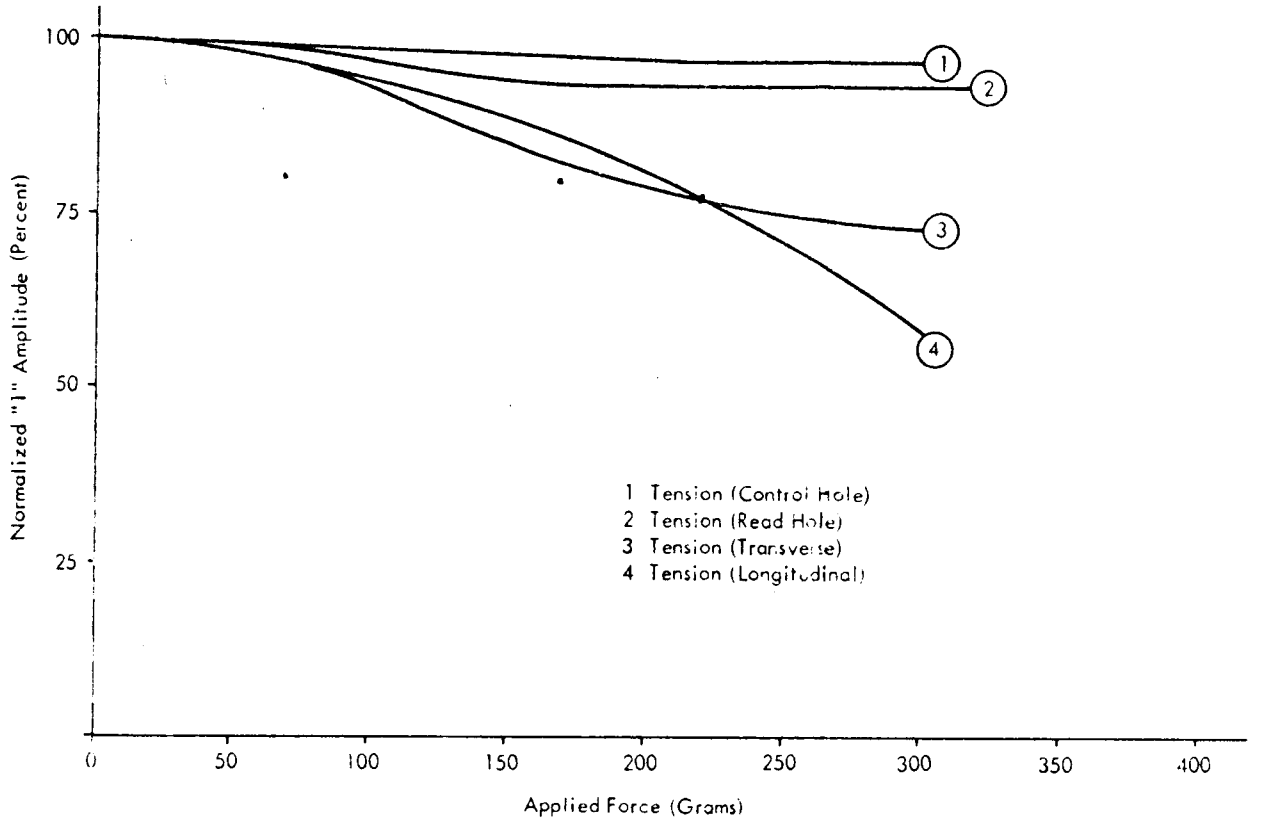


Figure 2-46. Results of MARS (T-39) Memory Core Test (Tension)

Two cores were then encapsulated and tested using the following encapsulants: GE Sylgard 183, Dow Corning A-4000, Dow Corning 630 and Laminar X-500 flexible. The electrical characteristics of the cores were determined at 10°C, 40°C and 70°C. The Sylgard showed no appreciable change in the undisturbed unit (1) response, peak time of the unit (1) response, and switch time of the unit (1) response. Dow Corning A-4000 caused complete degradation at 10°C, and Laminar X-500 caused a marked increase in switch time at the same temperature. Dow Corning 630 exhibited a significant degradation on all parameters at 10°C. GE Sylgard 183 silicone proved to be the best encapsulant in this test; Laminar X-500 (8C8/10C56) was second.

GE Sylgard 182 and 183, GE SS-4090, Laminar X-500 (8C8), and Conap 1132 were applied to array quadrants, and the cores were checked electrically. None of the cores coated with either Sylgard showed electrical degradation. However, GE SS-4090 and Laminar X-500 (8C8) caused some degradation. The effects of Conap 1132 depended on the cure cycle and ranged from no degradation to considerable degradation. The Conap is undergoing further testing.

h. Vacuum Stability of Encapsulants

The following encapsulants were applied to aluminum foil and then cured:

Encapsulant	Weight Loss (Percent)
Laminar X-500 (8C8)	2
GE SS-4090	2
Dow Corning 630	5
Conap 1132	(stopped at 80°C to 90°C)
Sylgard 182	2

The stability of each encapsulant was tested at 100°C and 10^{-8} in. Hg for 96 hours. Dow Corning 630 showed a 5 percent weight loss, while Laminar X-500 (8C8), GE SS-4090, and the Sylgards showed appreciable losses. The Conap 1132 is undergoing further tests because of the varying properties revealed during different cure cycles.

i. Vibration of an Unencapsulated Memory Plane

An unencapsulated square plane with toroid cores was vibration tested in the horizontal plane between 16 and 2000 cps at 5, 10 and 30 G's rms. The

memory plane's resonant frequency rose from 115 cps at 5 G to 200 cps at 30 G. Also, a sharp drop was noted in the amplitude of the center of the plane just beyond the resonant point of the plane. Both facts indicate a non-linear vibration. Transmissibilities of 14.6, 12.8, and 17.7 at the three resonant points, respectively, indicated a need for some form of damping.

j. Vibration of Encapsulated Memory Planes

Three square planes were wired with toroid cores and then encapsulated with Sylgard 182, GE SS-4090, and Conap 1132. The two planes encapsulated with Sylgard 182 and Conap 1132 were vibrated in the horizontal plane from 16 to 200 cps at 5, 10, 20, and 30 G's rms. This vibration produced no electrical degradation of the cores. The transmissibilities noted on the Sylgard-coated plane at 5, 10, and 17 G's rms (no reading could be obtained at 30 G) were 1.57, 0.855, and 1.65, respectively, at resonance (30 cps). The transmissibilities of the Conap 1132-coated plane were slightly lower than for the Sylgard-coated plane. At 5 and 10 G's no resonant point could be detected visually. At 20 and 26 G's a resonant point was observed between 60 and 70 cps; transmissibilities were 1.07 and 0.834, respectively.

The Sylgard and Conap-coated planes were then vibrated longitudinally at 5, 10, 20, and 30 G's rms from 16 to 2000 cps. No electrical degradation of the cores was noted, and no vibration ripples occurred in the plane.

The GE SS-4090-coated plane is now undergoing vibration testing. An array of these planes separated by foam spacers will also be vibration tested.

Because of the excellent response shown by Sylgard 182 in this and the other tests, this material will be used to encapsulate all computer memory planes. The Conap 1132 has some desirable properties, such as being removable for core repair and possessing good vibration and ease-of-fabrication properties, so work will be continued to determine the cure cycle which will give Conap 1132 minimum weight loss in vacuum but which will not affect the cores.

3. MATERIALS INVESTIGATIONS

a. Computer Structure

During the reporting period the Materials Laboratory constructed and welded a model of the hollow-walled, liquid-cooled magnesium-lithium structure for vibration tests. This unit was pressurized from 5 to 40 psi and subjected to a 6 G rms sinusoidal vibration between 20 and 2000 cps at sweep rates of 0.5 octave per minute in each of the three orthogonal axes. No degradation, structure fracture, or leaks were observed at any point on the model part.

These tests proved that (1) welded magnesium-lithium structures can meet Saturn V environmental vibrational requirements, and (2) the integrity of the welded joints will be maintained when the structure is subjected to both vibration and pressurization.

b. Pages

The Laminar X-500 was evaluated and found suitable for coating epoxy- and urethane-coated ULD's. A supported, modified epoxy, FM 96, made by the Bloomingdale Rubber Co., will be used to bond MIB's to the page frames. FM 96 was tested, with the following results:

- FM 96 was used as a bond between LA 141 and a fluoride-anodized, Laminar X-500-coated page frame. The bond to the LA 141 failed.
- The material will be acceptable in vacuum environment.
- Processing modifications are required to prevent FM 96 from flowing into MIB holes. A possible solution is to seal the MIB bottom prior to bonding.

c. Transfer Molding

Based on tensile bond strength tests, a phenolic and an epoxy material were selected for use in transfer molding. Two ULD's containing functional components were molded by each material. The materials adhered well, and components were not damaged. All samples passed initial thermal cycling tests. An additional 10 ULD's with functional components were then molded by each material. All epoxy ULD's passed the initial electrical tests, but some of the phenolic-coated ULD's failed. Eventually all of these test ULD's will be soldered to pages, thermally cycled, and electrically tested to assure that the materials are sound and meet required environmental conditions.

d. Magnesium-Lithium

(1) Corrosion

Frames constructed of bare magnesium-lithium and fluoride-anodized magnesium-lithium coated with Laminar X-500 have been corrosion-tested for 330 hours. No significant corrosion has occurred on either specimen. Test conditions consist of a mixture of 40 percent water and 60 percent methanol circulated through the fabricated sections at 0.5 gallon per minute at room temperature. Testing will continue for a total of 1000 hours. NASA has advised IBM that magnesium-lithium would be practical for application in the computer cooling system if careful attention is given to design details, such as corrosion protection and the use of dissimilar metals.

(2) Plating

A solution of 0.3 N sodium hydroxide containing 5 grams per liter of sodium fluoride was used to clean magnesium-lithium samples. The samples were then soldered together and sized into specimens for a lap-shear strength test. Although the tests showed that better adhesion was obtained than in previous tests, further improvement is required before this process can be considered satisfactory. This program will be continued unless it is definitely proven that magnesium-lithium cannot be soldered effectively.

(3) Welding

The mechanical strength and metallurgical properties resulting from Heli-arc welding of magnesium alloy sheets was investigated. The following conclusions were reached:

- The use of helium causes the liquid weld pool to appear cleaner than when argon is used.
- The LA 141 welding rod produced better mechanical and metallurgical properties than did the other welding rods used.

Additional samples of welded magnesium alloy satisfactorily passed the vibration test. Other welded structures successfully passed pressure tests.

(4) Fatigue testing

Pieces of LA 141 stock, 0.100-inch thick, were butt-welded by the Heli-arc process. The weld bead was then ground flush with the stock, and the specimens were stress relieved and straightened. The completed samples were then subjected to a stress ratio of -1 (reverse bending) for 2000 cycles per minute at 25 ± 5°C. After 10^7 cycles were completed the average fatigue strength of the welded specimens was 6500 psi as compared to 10,000 psi for unwelded LA 141 test samples.

e. MIB's

Micaply 102-11 underwent a two-fold investigation. First, information was obtained to determine the variables that would affect the MIB laminating cycle. Second Micaply 102-11 was compared with the present laminating material (Elson prepreg) to determine if Micaply 102-11 is suitable for MIB usage.

A study of Micaply flow properties indicated the following:

- The Micaply must be pressurized between 5 and 8 minutes (depending on board size) at 325°F to control resin flow.
- The rate of pressure application is critical; pressure should be applied at a slow uniform rate to assure even resin flow and air removal.
- The finished part should not be removed from the mold until the piece has been cooled,under pressure,to below 150°F.
- If the use of shims is eliminated from the lamination process, better resin flow and subsequent air removal are obtained.

Chemical studies of Micaply 102-11 indicate that the resin system comprises an Epon 1001-type epoxy and a dicyandiamide curing agent, the system used in Elson prepregnation. Both laminating materials are acceptable in the vacuum environment since weight loss is less than 2 percent. However, these materials failed the O_2 sniff test (ammonia odors caused by catalyst action were detected).

4. THERMAL ANALYSIS AND TESTS

a. Computer Thermal Analysis

Computer logic pages were thermally analyzed to determine the temperature gradient across each page. The clock generator page had a gradient of 30°F when a magnesium-lithium structure was used. This gradient can be reduced to 11°F by using aluminum.

The inverter ULD module which employs leadless semiconductors had a 4°F gradient. The voter device showed a 5.10°F gradient. Calculations indicate that approximately the same thermal profile can be expected for both the leadless and wire-lead type pages.

The over-all structure of the preliminary computer design underwent 7090 Computer analysis. This program is being continually updated.

b. Infrared Study and Measurement Program

Preliminary attempts were made to determine the K factors (°C per watt) of the component chip on the substrate by attaching a thermocouple (No. 40 AWG wire) to the chip.

Miniaturized thermistors, as well as an oil bath technique, were considered in this effort. But since these three methods were destructive and extremely inaccurate, they were abandoned in favor of nondestructive infrared techniques. The resolution of the optical system and the infrared detector in the radiometer have been improved such that the K factor can be accurately determined by this technique. These measurements will be made during October.

c. Oven Temperature Profile

Tests show that the oven used to fuse the semiconductor chips onto the ULD's will not exceed the maximum allowable temperatures of the ULD components.

d. Thermal Evaluation of the Page Retainer Clip (IBM No. 6110810)

The page retainer clip provides excessive thermal resistance to heat flow from the page to the computer wall. Multiple testing with and without interstitial materials in the interfaces verified that the clip design is undesirable. This study is discussed in IBM Report No. 544-045.

An alternate page clip which would give good heat transfer characteristics is being redesigned, based on satisfactory thermal results from a "wire mesh over rubber" technique. During tests this type of clip was soldered to the page and held the page by using grooves in the computer wall.

e. Thermal Evaluation of Rifle-Bored Heat Exchanger

Heat transfer coefficients were determined for various coolant flow rates through the proposed computer heat exchanger. Refer to IBM Report No. 544-037.

f. Pressure Drop Tests on Proposed Heat Exchanger Models

Comparison tests were run on both a finned coolant passage and drilled hole-type coolant passage. The pressure drop in the tubular type was less than 1/8 that of the finned passage. This task is summarized in IBM Report No. 544-034.

g. Thermal Evaluation of Finned-Passage Heat Exchanger

Heat transfer coefficients were determined for various coolant flow rates through the finned-passage heat exchanger. The evaluation is discussed in IBM Report No. 544-039.

h. Thermal Comparison Study of Finned and Tubular Heat Exchangers

The thermal characteristics of a finned and a tubular heat exchanger were compared by using test results and calculations. The tubular heat exchanger has slightly better unit heat rejection per unit pressure drop. Refer to IBM Report No. 544-047.

i. Fabrication of Thermal Mock-up

Hardware has been ordered for a computer thermal mock-up, which will be shipped to NASA. Work will progress as the hardware becomes available.

j. Over-All Computer Heat Transfer Analysis

The thermal characteristics of a computer operating in the expected Saturn V environment are discussed in IBM Report No. 561-001.

k. Design and Fabrication of Liquid Cooling System

A portable closed-loop liquid cooling system for laboratory thermal testing of the computer and data adapter unit is being designed. Hardware is now available for fabrication of the methanol system.

l. Reports

More detailed information on these thermal analyses and tests is available in the following reports:

IBM Report Number	Title
544-001	Weight Status Report
63-544-14	Weight Status Report
544-009	Trussgrid Thermal Evaluation
544-012	Weight Status Report
544-025	Weight Status Report
544-034	Pressure Drop Tests on Advanced Saturn Heat Exchangers
544-037	Thermal Tests on Rifle-Bored Heat Exchanger
544-038	Weight Status Reports
544-039	Thermal Tests on Finned Heat Exchanger
544-047	Comparison of a Finned vs. Tubular U-Shaped Heat Exchanger

IBM Report Number	Title
544-048	Weight Status Report
561-001	Analytical Heat Transfer Studies for Advanced Saturn

5. ELECTROMAGNETIC COMPATIBILITY

To date all r-f shielding efforts have been applied to the Saturn V system ground (Figure 2-47). Interface circuits have been studied, and cabling and wiring layouts and power conversion circuitry were sketched.

6. THEORETICAL ANALYSIS

a. ULD's

The stresses induced in ULD wrap-around joints were studied. Neither the Alpha 903 full-solder joint nor the CD mechanical clip functioned reliably in a theoretical 100°C thermal shock environment. Two mechanical clip configurations, in which relative substrate-to-MIB strain was taken up by clip bending, functioned well analytically.

b. Structural

A computer program for determining the natural frequency of beams has been completed. The program, applicable to nonoverhanging beams, can handle 50 discrete weights and 30 changes in moments of inertia of the beam along its length. The program handles the four possible cases ranging from completely built-in to completely simply supported. In addition to natural frequency, the program also computes static deflection and static stresses. By transferring the kinetic energy of internal members in the Saturn V units to the mounting beams, this program will be used to determine the dynamic stresses of the beams.

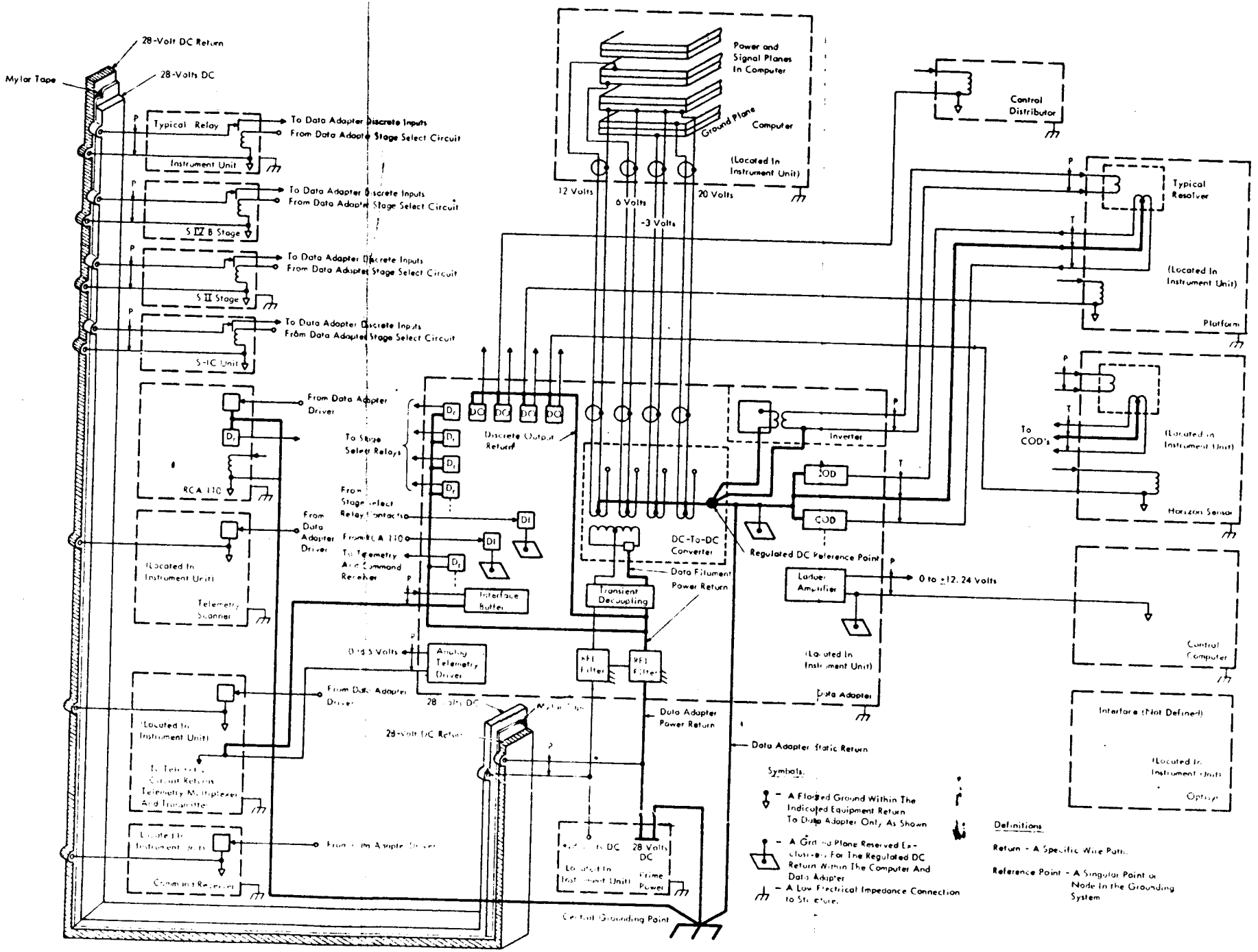


Figure 2-47 . Saturn V System Grounding Diagram

Section III

Laboratory Test Equipment

Section III

Laboratory Test Equipment

A. ELECTRICAL DESIGN AND TESTING

The Aerospace Computer Manual Exerciser (ACME) will perform the following basic functions with the Saturn V computer:

- Rapidly load, and verify the loading of, the Saturn V computer memory.
- Display the selected computer internal data and corresponding address information during performance of a demonstration or diagnostic program, with the computer operating separately from the remainder of the guidance system.
- Simulate the Saturn V Data Adapter in (1) operator-selected PIO data inputs to the computer and (2) receiving and displaying PIO data outputs from the computer.

In addition, the ACME will provide the computer all required d-c voltages, properly sequenced and regulated, as well as providing liquid heating or cooling, as necessary, to maintain the computer in the proper operating temperature range.

The ACME will use a modified Rheem Electronics Photoelectric Paper-Tape Reader and Spooler which is capable of reading 500 eight-bit characters (on an eight-track tape) per second. Each group of nine characters on the tape constitutes one tape word.

Each tape word will include 26 bits of data to be loaded or verified in a particular computer memory location and the necessary address and command information to cause the ACME and computer to do the desired loading or verification. Thus, the time required to load and separately verify the two 4096-word memory modules of one duplex pair (assuming no errors) will be less than 3 minutes 45 seconds. If the contents of a previously loaded memory should require verification, the "VERIFY ONLY" switch on the Tape Reader Control Panel will cause the load portion of the load/verify tape to be ignored. If an error is detected, the tape will automatically stop and cause the erroneous word and its address to be displayed. After manual correction

and verification via the appropriate switches on the Memory Loader/Data Display panel, automatic verification would be resumed. Manual loading and verification are possible at any time so that minor program modifications can be made quickly.

When the computer is operated with the ACME, data from internal computer data channels (e.g., Accumulator, Transfer Register, Product or Negative Remainder, etc.) may be selected at a particular point in the program, as determined by the instruction address or data address, and displayed with the corresponding selected address and instruction. As the computer operates, six data channels (which are among those normally displayed as described above) will be written into delay lines which are 13 instruction-cycle times long. Therefore, by either operator command or by automatic detection of an error, the computer is placed in Single-Step Mode, and the history-storage delay-line information is recirculated. This information may then be displayed via the "PAST/PRESENT" switch, the "WORD" switch on the ML/DD panel. With the "PAST/PRESENT" switch returned to "PRESENT" and any detected error having been reset, the computer may then be advanced by the operator in single-instruction-cycle increments or free-running, as desired.

When computer covers are off, or for any other reason that internal signals not normally displayed are made available, the Spare Probes may be used to display the desired data. The operator, knowing the characteristics of the signal to be examined, must set the "CLOCK", "BIT GATE", and "PHASE" switches on the Interface Exerciser (IE) panel to the clock, bit gate, and phase at which he wishes to sample the signal and begin shifting the data into the Data Display Register. These same three switches also generate a signal, in conjunction with the selected "PHASE", "BIT GATE", and "CLOCK", which is available as a marker or intensifier for oscilloscope use. When data or an instruction address compares, or the computer is advanced in the Single-Step Mode, a sync signal is produced for triggering an oscilloscope.

The capability of the computer to communicate with the data adapter will be tested and used by the IE. When the computer program calls for a PIO operation, data from the computer accumulator and memory will be received by and displayed from two registers in the IE, or received by the computer accumulator from one of the two ACME IE registers, as selected by the program. Since the operator can preset the IE registers, he can control the logical choices within the computer during the performance of a suitable program, and thus select subroutines. The switches on the ACME IE panel, and the relays within the ACME, control the power supplied to the TMR computer voter circuits, and the circuits driving them, to allow the selection of one channel of the computer or one channel of any computer module by forcing the other two channel outputs to a logical "1" and a logical "0". While a channel or module is being selected, the computer will be stopped by the control signal, HLT, and until a proper "path" has been selected, the operator will be unable to start the computer.

Every effort is being made to make the ACME easy to maintain and repair. A "LAMP TEST" switch on each ACME panel will allow the operator to check all lamps easily. Error-detection circuits and appropriate indicators in the ACME will alert the operator, should any trouble occur and, in many cases, give him a good indication as to the cause and location of the trouble. Furthermore, the use of a self-check tape, internal self-check logic and the ACME/COMPUTER interface cables (disconnected from the computer and connected back to the ACME through special self-check connectors) will accelerate and facilitate troubleshooting of the ACME or verification of its ability to operate properly.

Eleven special circuit types will be required for the ACME to perform its required tasks with the Saturn V computer. These circuits have among their functions the translation of signals from computer logic levels to those of the ACME logic and vice-versa, the monitoring of computer disagreement detectors and the buffered computer clock oscillator ($\overline{BO}$), and the monitoring of thermistors within the computer package to be able to shut down computer power, should external temperatures go too high. Work on all 11 circuits has been underway for the past 4 months. Electrical design and testing of 10 of these circuits has been completed. Packaging is also well along.

The ACME power distribution and grounding schematics are 90 percent complete; component ordering for this portion of ACME is 99 percent complete. With the exception of some self-check logic, the ACME logic design is completed and ALD preparation is proceeding rapidly toward completion. The ACME schematics are 80 percent complete.

B. MECHANICAL DESIGN AND FABRICATION

The over-all mechanical design of the ACME is 85 percent complete; assembly is 30 percent complete.

1. CABINET

The three ACME cabinet frames (see Figure 3-1) are of a welded-unit construction with removable side covers. Interlocks have been used to cut off power when these covers are removed. The doors which provide access to the 10 power supplies have been hinged on one side and are also interlocked as a safety precaution. All frames are mounted on casters, and caster locks have been provided on the computer test stand to immobilize this unit during computer handling.

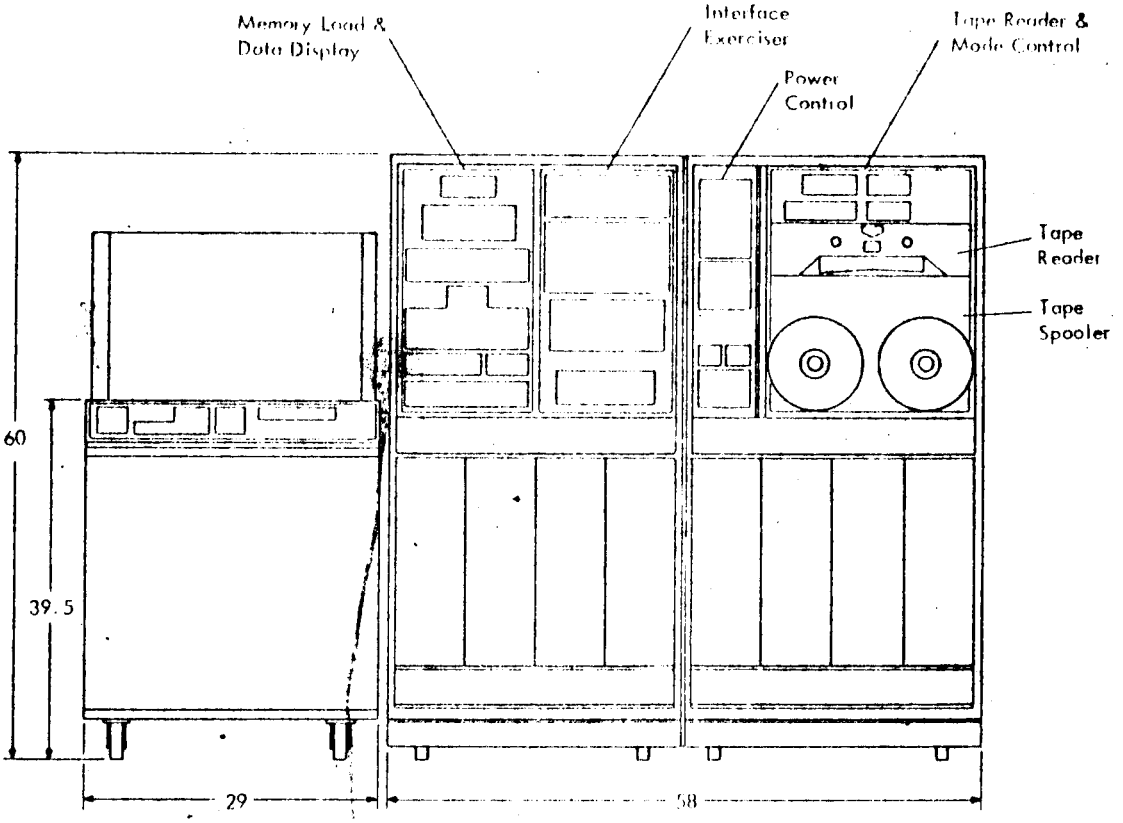


Figure 3-1. ACME Outline Drawing

2. OPERATOR PANELS

Operator panels (see Figures 3-2, 3-3, 3-4, and 3-5) have been organized with the functional areas finished in dark grey and a contrasting light grey for the background; the functional areas have been painted and nomenclature has been applied. The Memory Loader and Interface Exerciser panels are hinged on one side for maintenance, and the smaller Power Control and Temperature Modulation panels are fixed with screw type hold-downs.

3. TAPE CONTROL SYSTEM

A Rheem Photoelectric Paper-Tape Reader and Tape Spooler (see Figures 3-6 and 3-7) have been integrated to form the tape control system. The input medium is an eight-channel punched tape. The system is capable of a reading speed of 50 inches per second and is bidirectional for forward and

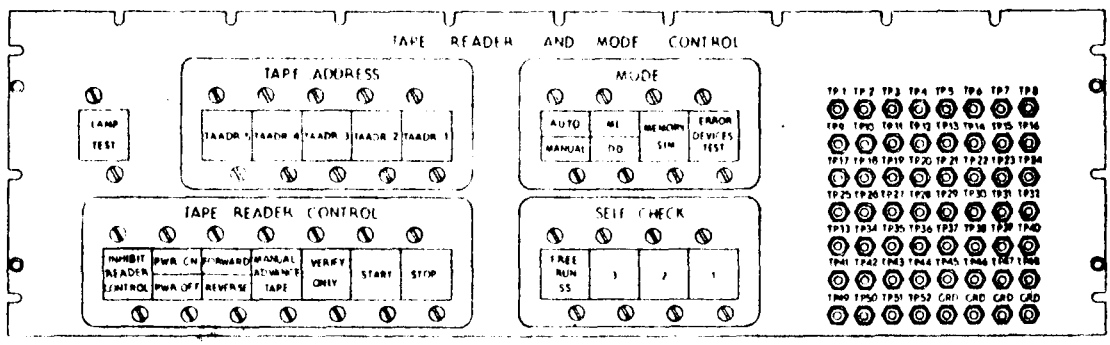


Figure 3-2. Tape Control Panel

reverse operations. The reel on the Spooler holds 1300 feet of plastic-base tape, 1 inch wide and 0.0026 inch thick. The Reader, Spooler, and Tape Control panel are slide mounted.

4. PRINTED-CIRCUIT CARDS

The "Translate" circuit has been packaged on printed-circuit cards compatible with the standard line designed, built and tested in the General Products Division of IBM. This printed-circuit is illustrated in Figures 3-8 and 3-9.

5. LOGIC CHASSIS GATES

The logic chassis which contain the circuit cards and components are hinged on one side for ease of accessibility in checkout, maintenance, and modification activities. There are 11 gates containing approximately 1300 logic cards. A blower is mounted on each chassis for cooling components.

6. DELAY LINE GATE

Three delay lines and associated logic are mounted on a hinged gate. Delay lines and logic components are air-cooled with blowers mounted on the bottom of the chassis.

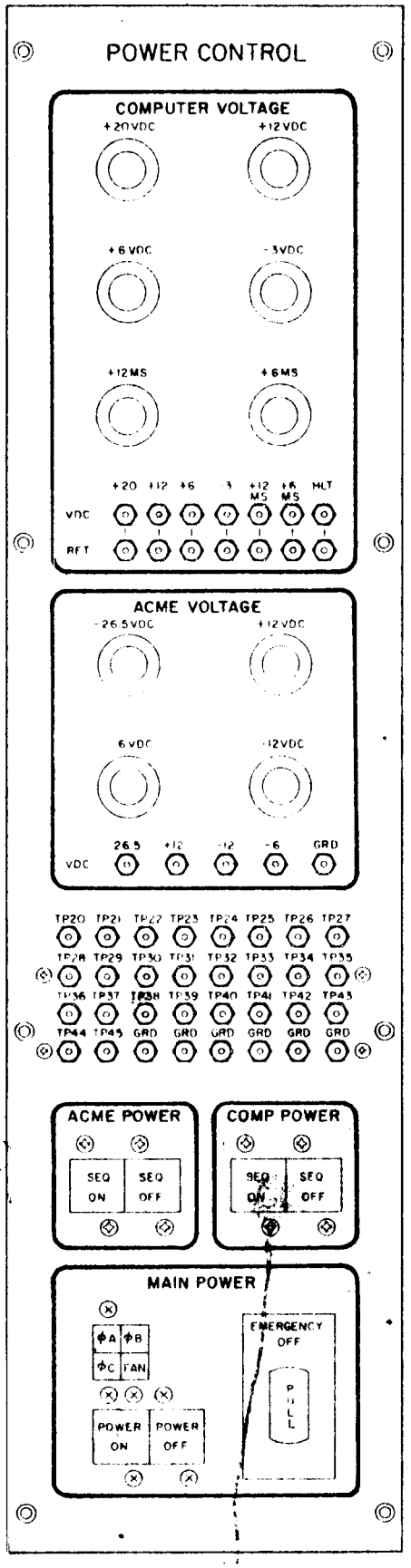


Figure 3-3. Power Control Panel

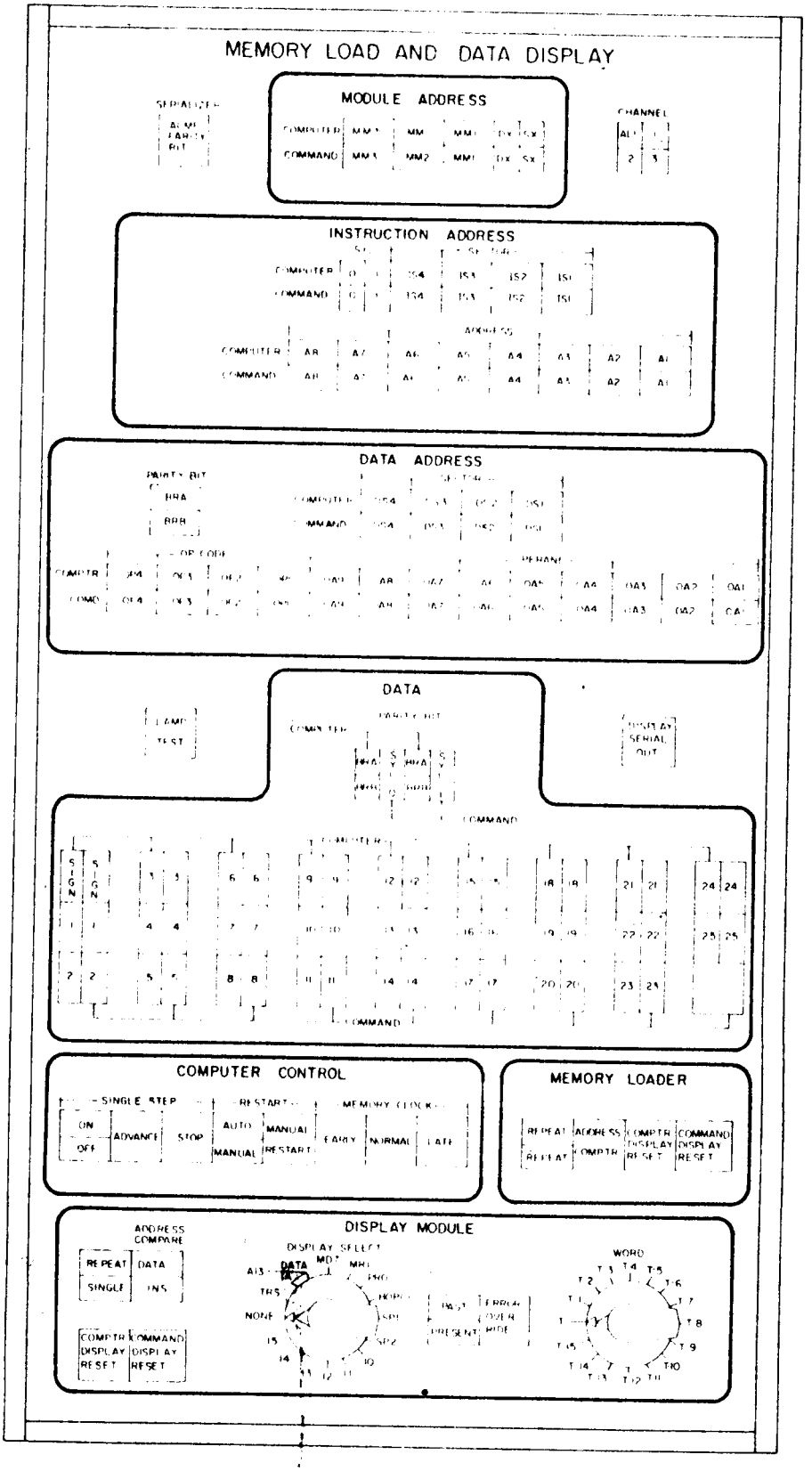


Figure 3-4. Memory Load/Data Display Panel

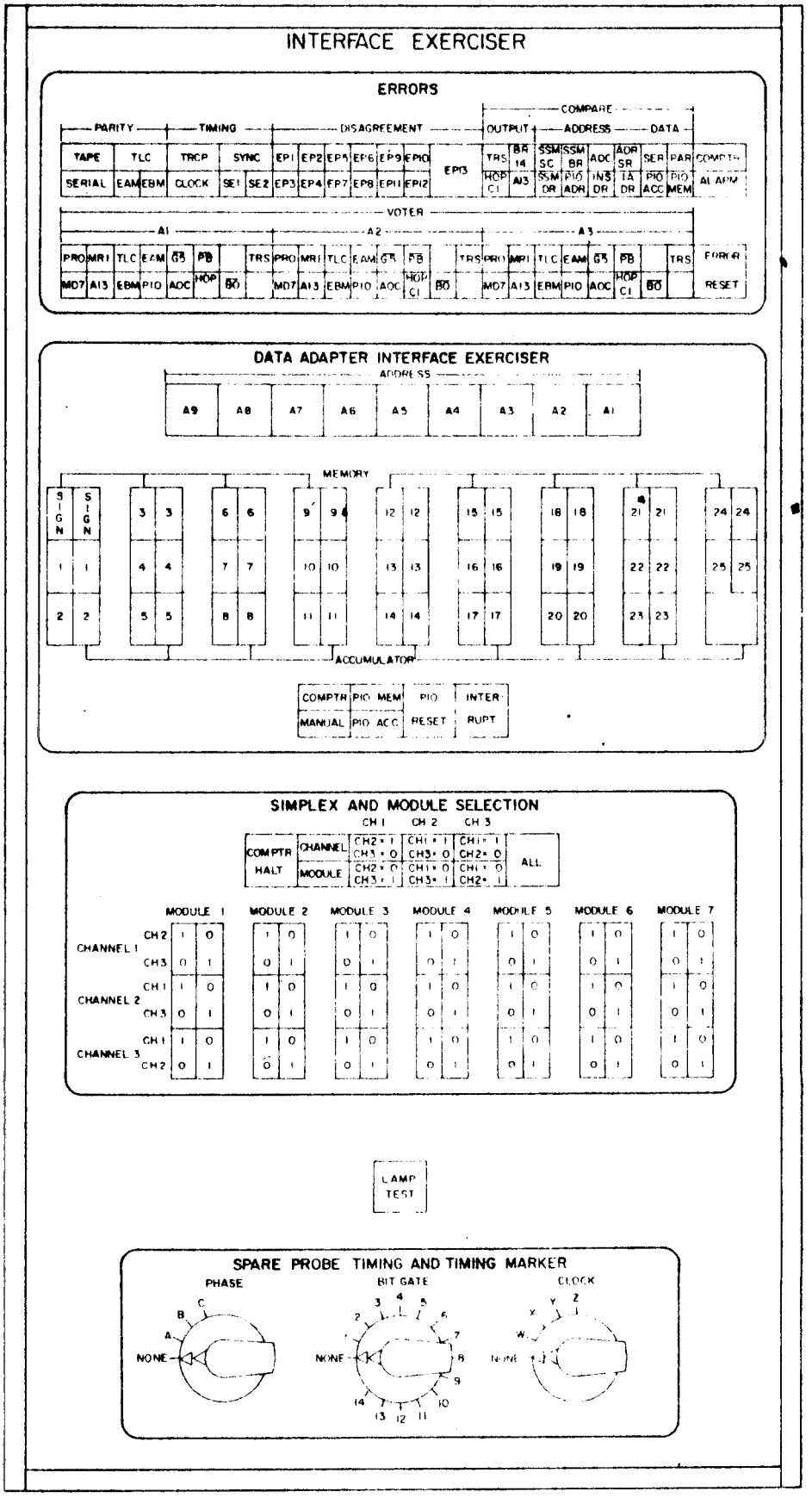


Figure 3-5. Interface Exerciser Panel

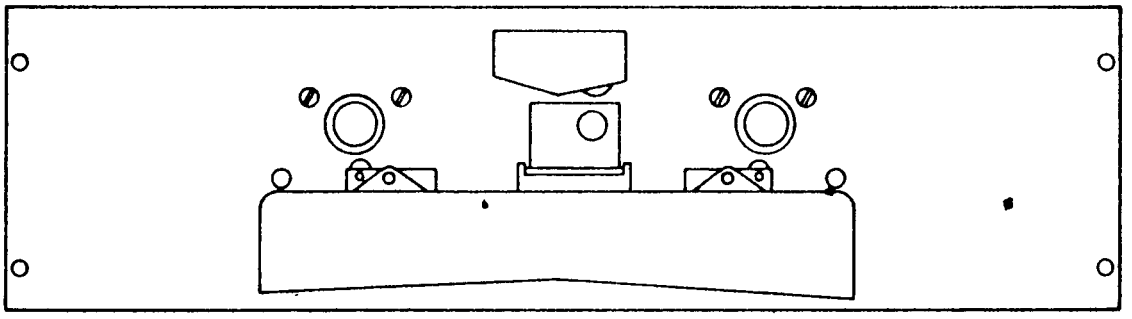


Figure 3-6. Tape Reader

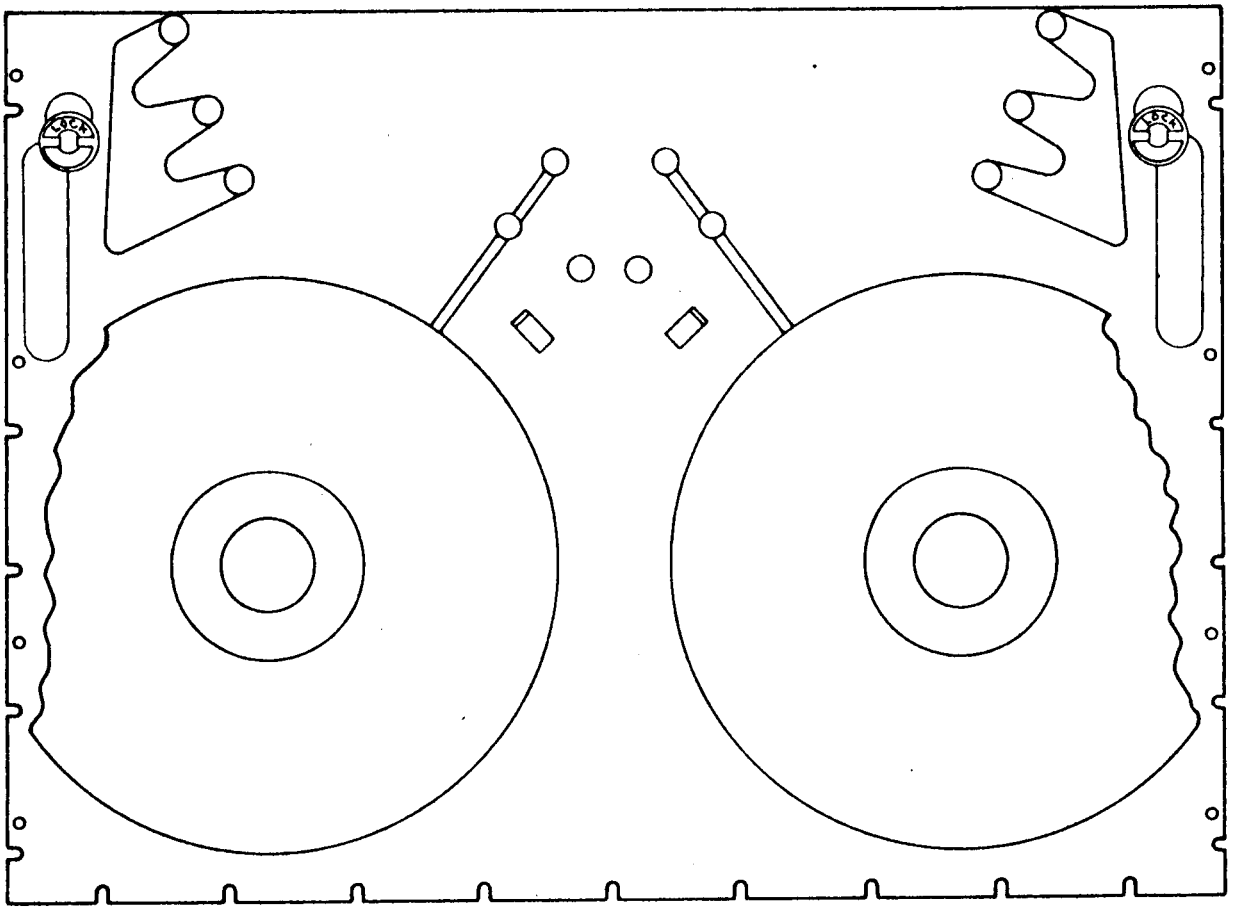
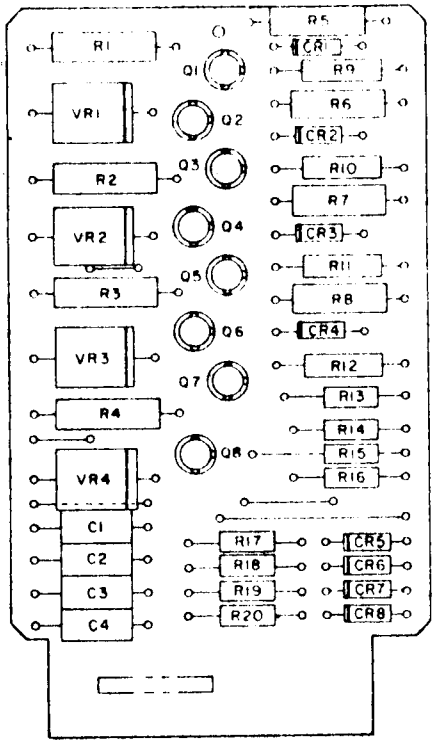
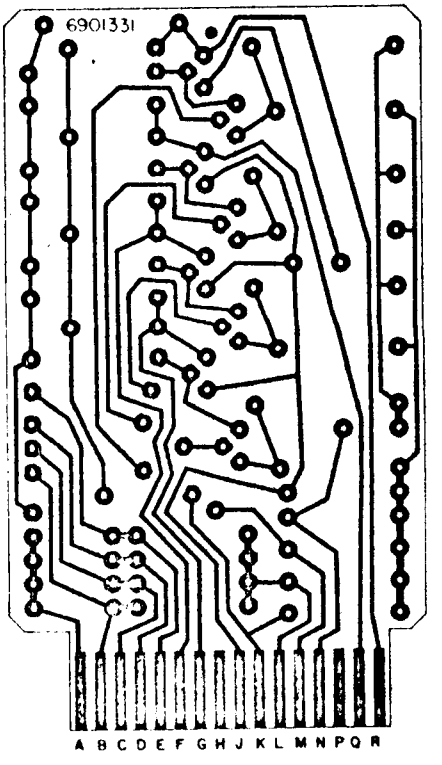


Figure 3-7. Tape Spooler



A. Component Side



B. Wiring Side

Figure 3-8. "Translator" Printed Circuit Board Assembly

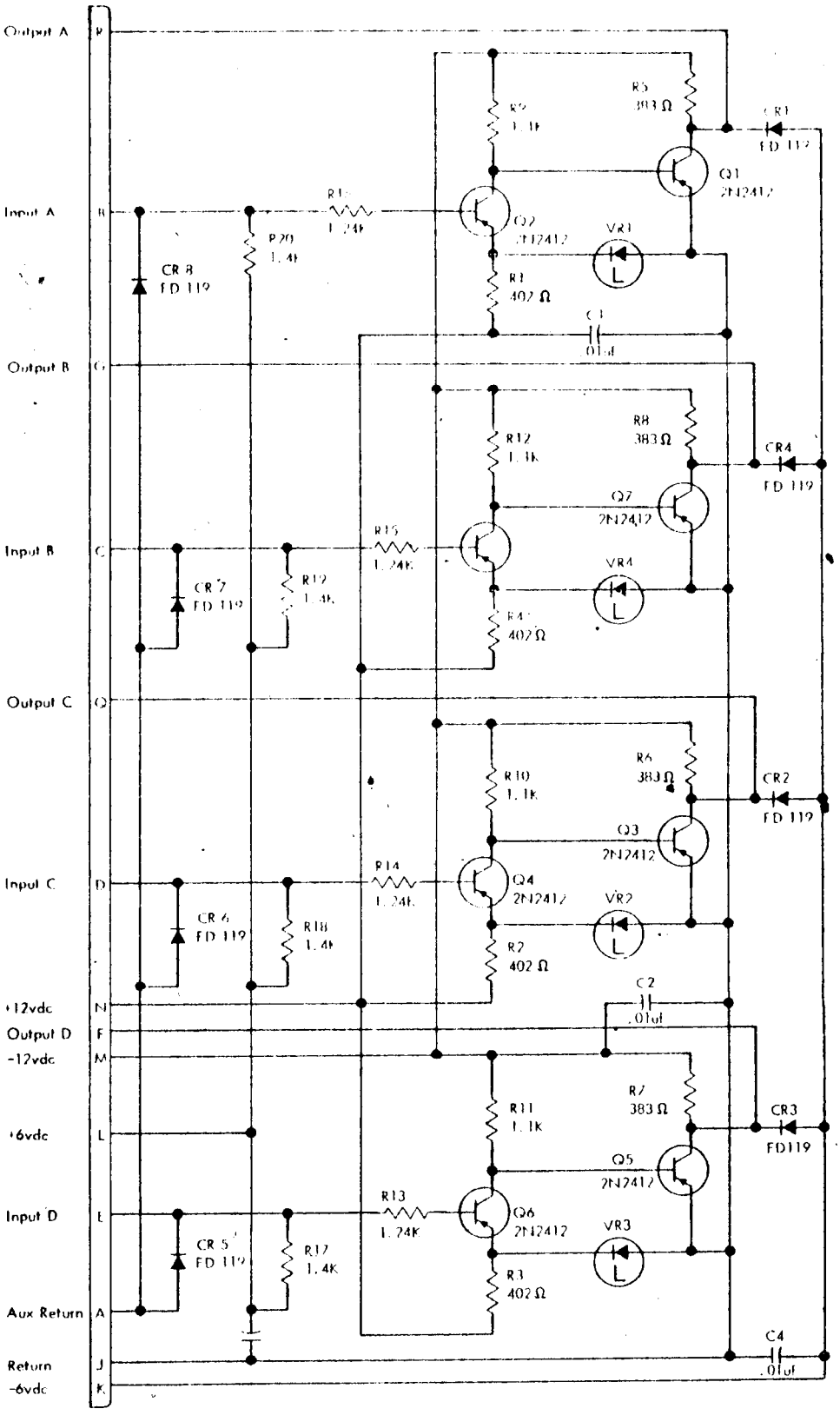


Figure 3-9. "Translator" Schematic Diagram

7. POWER SEQUENCING RELAY GATES

Two hinged gates are used to house relays for power sequencing. One gate contains those relays used for power sequencing within the ACME unit and the other contains those used for computer power sequencing.

8. MODULE SWITCHING GATE

This gate, typical of the ACME power sequencing, computer power sequencing, and delay line gates, contains 37 eight-pole relays. The AC Power Box within this gate contains transformer, circuit breaker, and power contactor relays, and an elapsed-time indicator. As a safety precaution, removal of the module side cover is necessary to reset the circuit breakers.

9. INTERFACE CONNECTOR PANEL ASSEMBLY

Four 55-contact connectors, three 61-contact connectors, and two 21-contact connectors are provided for computer connections on the interface panel. In addition, there are four 55-contact connectors, four 61-contact connectors, and one 16-contact connector used during ACME self-check. There is only one 16-contact connector which connects the ACME electronics unit to the computer test stand. Fifty-five test points, and four test jacks and load resistors, complete this subassembly.

10. COMPUTER TEST STAND

The computer test stand houses the computer temperature modulator and retains the computer holding fixture. The computer temperature modulator consists primarily of a circulating pump, hot and cold sumps, a heat exchanger, a condenser, and relay-controlled solenoids.

The cooling system will use distilled water as a cooling agent for the computer when it is operational. The system shall provide a minimum flow rate of 12 pounds per minute and has the capacity to cool the computer and the adapter individually and collectively during tests.

If an overheat condition is reflected by a computer thermister, computer power will be shut off and an overheat indicator light will be illuminated.

Fabrication of the test stand is approximately 60 percent complete. Working drawings are approximately 80 percent complete and work is proceeding on schedule.

Section IV

Reliability

Section IV

Reliability

A. INTRODUCTION

The component-part failure rates used to predict the reliability of the Saturn V computer are based on field and test data collected during various IBM guidance computer development programs. However, in those cases where the developmental nature of the components preclude having data available to draw upon, the estimated failure rates are based on engineering judgment.

Saturn V component failure rates are listed in Table 4-I. Rates are provided for surface or junction temperatures of 100°C, 70°C, and 60°C. In all cases, these rates assume a benign mechanical environment.

For the boost phase of the mission, these failure rates will increase an estimated 50 times. In addition, the conditional possibility of an "open" during the boost phase is assumed to be 1.0.

During the past 6 months, more versatility has been introduced into the reliability prediction methods used for Saturn V. The IBM 7090 Computer Monte Carlo program for predicting reliability has been made more complete by adding a multiple-phase mission prediction capability, wherein each phase of a given mission can have different times, component part failure rates, and component part conditional failure probabilities.

Thus the 7090 Computer Monte Carlo program can analyze the launch phase as well as the orbital phase of the mission.

The following additional reliability computations are now performed by computer programs:

(1) Adjustment of component failure rates to account for associated mounting and interconnecting hardware in the TMR machine.

(2) Confidence limits for the Monte Carlo reliability determination.

Table 4-I

Saturn V Component Part Failure Rates

Component Type	% of Rated Electrical Stress	Failure Rates at Various Temperatures					
		100°C		75°C		60°C	
		$\lambda \times 10^6$	K_o*	$\lambda \times 10^6$	K_o*	$\lambda \times 10^6$	K_o*
TRANSISTORS							
Leadless	≤ 10	0.016	0.28	0.014	0.32	0.012	0.38
Leadless, matched pair	≤ 10	0.048	—	0.042	—	0.036	—
Silicon, planar, in stitched, welded can	≤ 10	0.016	—	0.013	—	0.011	—
Silicon, planar, in stitched, welded can	≤ 50	0.026	—	0.02	—	0.017	—
Silicon, planar, matched pair, in stitched, welded can	≤ 10	0.048	—	0.039	—	0.033	—
Silicon, planar, matched pair, in stitched, welded can	≤ 50	0.078	—	0.06	—	0.051	—
Silicon, alloy, power	≤ 50	0.2	0.1	0.16	0.1	0.14	0.1
DIODES							
Dual, leadless, half used	≤ 10	0.009	0.33	0.007	0.42	0.007	0.46
Dual, leadless, both halves used	≤ 10	0.008/half	0.33	0.006/half	0.42	0.006/half	0.46
Zener, discrete	≤ 50	0.1	0.33	0.08	0.33	0.06	0.33
Silicon, planar, micro.	≤ 10	0.01	—	0.009	—	0.008	—
Silicon, power rectifier	≤ 50	0.15	0.1	0.12	0.1	0.1	0.1
RESISTORS							
Cermet (ULD type)	≤ 30	0.018	0.72	0.015	0.72	0.013	0.72
Metal film, precision	≤ 30	0.03	0.99	0.026	0.99	0.022	0.99
Molded, carbon comp., nonhermetically sealed	≤ 30	0.005	0.99	0.004	0.99	0.003	0.99
Variable trimmer	≤ 10	0.18	—	0.16	—	0.15	—
Temperature-sensing, memory	—	0.001	—	0.001	—	0.001	—
CAPACITORS							
Glass	≤ 10	0.003	0.99	0.002	0.99	0.001	0.99
Ceramic	≤ 30	0.03	0.5	0.02	0.5	0.015	0.5
Tantalum, solid section	≤ 50	0.1	0.1	0.08	0.1	0.06	0.1
CONNECTIONS							
Unit or page connector body	—	0.003	1.0	0.003	1.0	0.003	1.0
Active connector pins, per pair	—	0.007	0.8	0.007	0.8	0.007	0.8
Flow solder	—	0.001	1.0	0.001	1.0	0.001	1.0
Hand solder, memory frame	—	0.0005	1.0	0.0005	1.0	0.0005	1.0
Solder fillet (ULD)	—	0.001	1.0	0.001	1.0	0.001	1.0
Hand solder, memory address wire	—	0.0002	1.0	0.0002	1.0	0.0002	1.0
Sense or inhibit wire	—	0.00028	1.0	0.00028	1.0	0.00028	1.0
Splice	—	0.00036	1.0	0.00036	1.0	0.00036	1.0
Chip to conductor, pattern/ball	—	0.0005	1.0	0.0005	1.0	0.0005	1.0
OTHERS							
Core, toroidal, T-38	—	0.0001	—	0.0001	—	0.0001	—
Cable, flexible, tape, per length	—	1.0	0.9	1.0	0.9	1.0	0.1
Choke, filter, power	≤ 50	0.15	—	0.13	—	0.12	—
Choke, R.F.	—	0.1	—	0.1	—	0.1	—
Crystal, oscillator	—	0.5	—	0.5	—	0.5	—
Delay lines, glass	—	0.3	—	0.3	—	0.3	—
P.C. Strip, memory	—	0.0001	—	0.0001	—	0.0001	—
MIB (1 page side)	—	0.553	0.80	0.553	0.80	0.553	0.80
MIB (back panel)	—	3.76	0.80	3.76	0.80	3.76	0.80
Transformer, signal	≤ 50	0.5	0.99	0.45	0.99	0.43	0.99
Transformer, pulse	≤ 50	1.0	0.99	0.8	0.99	0.7	0.99
Wire, memory, per wire	—	0.0001	1.0	0.0001	1.0	0.0001	1.0
Transformer, pulse	—	0.16	—	0.16	—	0.16	—
"H clip", including joint to land pattern	—	0.0005	1.0	0.0005	1.0	0.0005	1.0
Wrap-around land, ULD	—	0.0005	1.0	0.0005	1.0	0.0005	1.0
ULD conductor pattern	—	0.0001	0.6	0.0001	0.6	0.0001	0.6
Substrates	—	0.0001	1.0	0.0001	1.0	0.0001	1.0

*K_o conditional probability of failure by the open mode.

(3) Simplex reliabilities for certain logic groups, such as a single channel of the TMR machine, and the clock generation for each channel.

(4) Reliability of the combination of TMR logic and clock generation, with confidence limits on the resulting system reliability.

(5) Memory reliability calculations including launch-phase factors.

B. COMPUTER RELIABILITY ANALYSIS

The estimated reliability of the Saturn V computer is based on a mission length of 250 hours following an 11-minute launch period. Operating junction temperatures are assumed to be no greater than 60°C. Two additional estimates, for missions of 100 and 500 hours, are given to illustrate the nonlinearity of the reliability curve for equipment built using redundancy techniques. The 500-hour estimate is also an estimate for a 250-hour mission wherein all component-part failure rates doubled; similarly, the 100-hour number represents a 250-hour mission with all component part failure rates reduced to 40 percent of the predicted value.

The reliability model and system analysis technique used for these predictions are essentially the same as those portrayed in the Saturn V Reliability Assessment Report (IBM No. 63-394-062). Differences are primarily the result of changes in usage or failure rates. For example, in the memory, hand soldered joints are now being used instead of flow soldered joints, and the failure rate for MIB's has been reduced as the result of reevaluation. (This change is explained in the appendix.)

The results of calculations for each block of the reliability model (see Figure 4 - 1), together with the reasons for any changes that have occurred since the aforementioned report was published, are contained herein. The technique of calculation is described in the initial Saturn V assessment report.

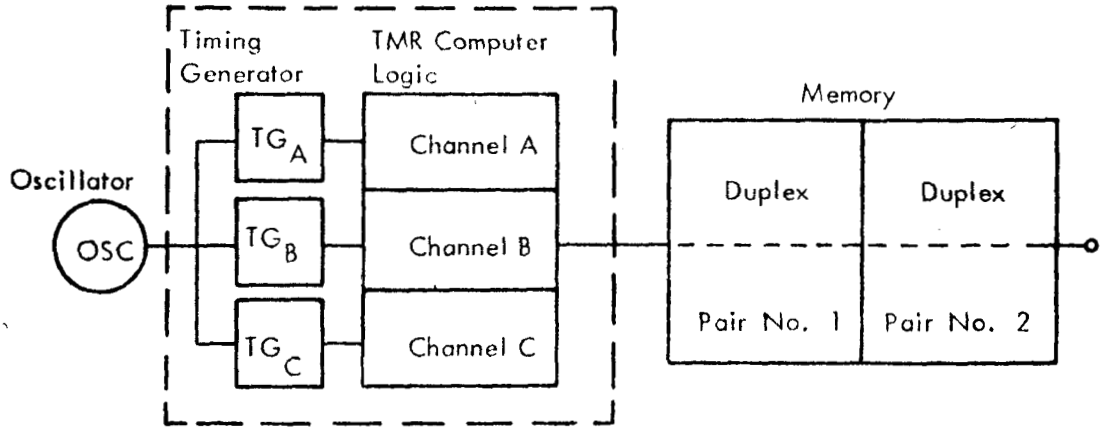


Figure 4-1. Computer Reliability Model

C. SUBSYSTEM CALCULATIONS

(1) Oscillator (no change)

(a) Simplex failure rate: 0.528×10^{-6}

(b) Oscillator reliability

1) 100 hours: 0.999947
2) 250 hours: 0.999868
3) 500 hours: 0.999736

(2) Computer Logic

(a) Digital logic reliability is obtained with a Monte Carlo program. The basic failure rates are adjusted to account for hardware utilized; the adjustment is described in Appendix A. The results of this analysis are given in Table 4-II.

Table 4-II

Computer Logic Reliability

Mission Time (hrs)	TMR Reliability	Simplex Reliability
100	0.9998	0.9877
250	0.9994	0.9716
500	0.9982	0.9439

(b) Timing generation: TMR logic reliability is somewhat compromised by timing. This problem is handled analytically by making the slightly pessimistic assumption that all timing for a single channel is serial to that channel, and by substituting appropriate values in the following equation:

$$R_{CL} = R_{TG}^{3} R_{TMRL} + 3 R_{TG}^{2} (1-R_{TG}) R_{SL}^{2} \qquad (1)$$

where

R_{CL} = Reliability of clock generation and logic.

R_{TG} = Reliability of serial clock generator.

R_{TMRL} = Reliability of TMR logic (from Table IV-2).

R_{SL} = Reliability of one serial channel of the three TMR channels.

These results are tabulated in Table 4-III.

Table 4-III

Clock Generator and Logic Reliability

Mission Time (hrs)	R_{TG}	R_{TMRL}	R_{SL}	R_{CL}
100	0.99856	0.9998	0.98331	0.999652
250	0.99641	0.9994	0.95879	0.998505
500	0.99284	0.9982	0.91927	0.994806

Differences between this and the previous assessment are due to more accurate circuit counts, hardware counts, and the changed MIB failure rate. The counts used to obtain R_{TG} and R_{SL} are tabulated in Appendix A.

(3) Memory

The minor changes in the memory numbers are due to the use of hand-soldered rather than flow-soldered joints, and to the change in MIB failure rate. Table 4-IV tabulates memory reliability.

Table 4-IV

Memory Reliability

Mission Time (hrs)	4000-word Nonredundant Memory	4000-word Dual Memory	8000-word Dual Memory
100	0.99239	0.99963	0.99927
250	0.98108	0.99888	0.99776
500	0.96252	0.99711	0.99424

D. SYSTEM ANALYSIS

Table 4-V summarizes the redundant system analysis; Table 4-VI gives a comparative summary of the equivalent simplex system.

Table 4-V

Redundant Computer Reliability

Subsystem	100 hrs	250 hrs	500 hrs
Oscillator	0.999947	0.999868	0.999736
Computer, clock and logic	0.9998	0.998505	0.994806
Memory (8000-word, dual redundant)	0.99927	0.99776	0.99424
Total Computer	0.99902	0.99614	0.98882

Table 4-VI

Nonredundant Computer Reliability

Subsystem	100 hrs	250 hrs	500 hrs
Oscillator	0.999947	0.999868	0.999736
Computer, clock	0.99856	0.99641	0.99284
Computer, logic	0.9877	0.9716	0.9439
Memory (8000-word, non-redundant)	0.98484	0.96061	0.92645
Total Computer	0.97127	0.92986	0.86798

E. ERROR DETECTORS

No redundancy is used in the hardware associated with error detection in the computer. Failure in these circuits is assumed not to be chargeable against computer reliability, since the equipment's capability to perform the mission is unaffected (i.e., the probability that failure in the error detectors will cause a system failure during a 250-hour mission is 2.27×10^{-9}, and is therefore considered insignificant). The following table lists the probability of success of the computer error detector circuits as a function of mission time.

Mission Time (hrs)

100	250	500
0.99753	0.99383	0.98766

F. SPECIAL RELIABILITY STUDIES

Several studies were performed to assist in making design decisions, and in evaluating the effect of certain critical elements on computer reliability. The numbers presented in this section may not, in some cases, represent the numbers as presently predicted due to changes in the prediction since the studies were performed. The conclusions drawn are, however, valid.

1. VOTER INTERFACE BETWEEN LOGIC AND MEMORY

The interface between TMR logic and dual redundant memories presents a problem with respect to the manner of going from three lines to two. The simplest technique is to use two conventional voters to vote on the trio of logic signals, and then use the output of each voter for one of the memories.

Voter failures are reflected either as failures in the TMR logic or as memory circuit failures. The first class of failures is easily analyzed as a part of the 7090 Monte Carlo program.

The effect of failures that are reflected as memory circuit failures depends on the effectiveness of the memory parity check and half-select current monitoring techniques.

If it is assumed that one-half of the expected first failures in the TCV and terminating resistors are detected by parity checking and half-current select monitoring, the TMR voter configuration will result in a predicted dual memory reliability of from 0.9984 to 0.9983 for a 250-hour mission (58 signals).

If one-half of the expected first failures in the TCV terminating resistors and only one-half of the EI short failures can be detected, the TMR voter configuration will degrade the predicted dual memory reliability from 0.9976 to 0.9965. Both of these analyses consider only one set of dual memories.

These analyses indicate that the proposed interface method is satisfactory from the reliability standpoint if the assumptions described for the first case are valid. This interface voting technique is included in the computer analyses presented in this report.

2. TIMING RELIABILITY

The present four-component timing oscillator is predicted to have a 250-hour reliability of 0.999868 at 60°C. The oscillator lowers the computer reliability from 0.995703 (assuming a perfect oscillator with R = 1.0) to 0.995571. Use of the oscillator is justifiable, then, insofar as it has a negligible impact on computer reliability.

To evaluate the merits of voting on the clock signals, three cases are considered:

Case I : No voting on clock signals (the present configuration).

Case II : Voting of the timing generator output (i.e., the clock driver input).

Case III: Voting at the clock driver output.

Reliability estimates for a 250-hour mission, assuming a junction temperature of 60°C, are:

Case I : $R = 0.9924$

Case II : $R = 0.9926$

Case III: $R = 0.9930$

Case III is impractical to implement due to the high current levels present at the clock driver outputs. The small reliability advantage of Case II over Case I indicates that voting at the clock driver input is ineffectual.

3. EFFECT OF FAILURES PRIOR TO LAUNCH

There may be occasions when launch of a Saturn V vehicle would be considered despite the existence of a failure in the redundant computer elements. The probability of mission success (reliability) then becomes a function of the location of the failed part. Four cases are considered:

Case I Failed part in computer TMR logic
Case II Failed part in timing generation equipment
Case III Failed part in memory
Case IV Failed part in power supply

The reliability of the computer and data adapter when no failures are present is 0.9924 for 250 hours at 60°C, as estimated in the initial reliability assessment.

a. Case I

The impact of a failure in the computer's TMR logic would depend on the location of the failure. However, an approximation can be obtained by assuming that the computer consists of seven equally reliable modules. In obtaining

a system reliability of 0.9924, an R_{TMRL} of 0.9989 was employed. This implies a trio reliability of

$$R_{TRIO} = (0.9989)^{1/7} = 0.99984$$

and

$$R_{MOD} = 0.9927$$

where

$$R_{TRIO} = 3 R_{MOD}^2 - 2 R_{MOD}^3$$

and

$$R_{TMRL} = (R_{TRIO})^7.$$

If a failure exists in one of the modules,

$$R_{TMRL} = (R_{TRIO})^6 R_{MOD}^2 = 0.9845$$

Having this value for R_{TMRL}, R_{CL} is computed. With the failure present, the equation becomes

$$R_{CL} = R_{TG}^3 R_{TMRL} + 2 R_{TG}^2 R_{SL}^2 (1 - R_{TG}) = 0.9818$$

This leads to a system reliability of

$$R_{SYS} = 0.9760$$

as compared to

$$R_{SYS} = 0.9924$$

with no failures present. This approximation portrays only non-voter failures in that the above equation for R_{TMRL} implies that the component failure disables only one module. A voter failure may well fail more than one module, but this situation would be recognized through failure indications by more than one disagreement detector. The approximation given, then, depicts the approximate probability of success given a failure indication from one disagreement detector.

b. Case II

If a failure is present in one of the three timing generation circuits, the reliability of the computer logic and timing generation is

$$R_{CL} = R_{TG}^2 R_{SL}^2 = 0.9048$$

Substituting this value of R_{CL} into the system equation yields

$$R_{SYS} = 0.8995$$

which again is compared to a "no-failure-present" reliability of 0.9924.

c. Case III

An 8000-word memory consists of two 4000-word, 28-bit memory systems, both of which must work for mission success. Each 4000-word system, in turn, contains two 4000-word memories arranged in a dual redundant configuration. Since the majority of possible memory failures would disable one of the memories in one of the 4000-word systems, mission success would then require operation of one duplex 4000-word system and one simplex 4000-word memory.

$$R_{MEM} = R_{4K\ \text{duplex}} \times R_{4K\ \text{nonredundant}} = 0.9777$$

Inserting this into the system equation gives

$$R_{SYS} = 0.9726$$

again as compared to 0.9924 with no failures present.

d. Case IV

If a failure is present in a power supply, success would require operation of five duplex supplies and one nonredundant supply. This leads to

$$R_{PS} = 0.99912$$

and

$$R_{SYS} = 0.9915$$

Thus, the extreme possibilities are Case II, in which the system reliability is reduced to 0.8995, and Case IV, where a reliability of 0.9915 is estimated.

4. DISAGREEMENT DETECTOR RELIABILITY

Each of the 169 disagreement detectors (DD) is predicted to have a failure rate of 0.14×10^{-6} failures/hour. This results in a predicted reliability of 0.99996493 for 250 hours, as compared to an average module reliability of 0.9927. The disagreement detector inverters (DDI's) are not included in the above numbers. The failure rate and reliability of each of the 13 DDI's are predicted to be 0.075×10^{-6} failures/hour and 0.999981, respectively.

The effects of failures in DD's and DDI's can be put into the following classes:

(a) No module failure exists, but a failure is indicated by one or more disagreement outputs.

(b) Module failures exist, but no failure is indicated.

(c) Module failures are caused by failures in DD's or DDI's.

(d) System failure is caused by failures in DD's or DDI's.

The probability of occurence of the four classes of events listed above are shown below for a 250-hour orbital mission. As a first approximation, it is reasonable to assume that the results are equally applicable to a 10-day period of operation prior to launch.

Class	Probability of Occurrence
1	0.000475
2*	0.000712
3**	0.001186
4	0.002276×10^{-6}

* This number includes the conditional probability that one or more module failures exist. If one were to define class (b) events as "One or more DD's and/or DDI's are incapable of detecting a module failure," the probability of a failure being present is approximately 0.127.

**This number does not include those combinations of module failures which cause system failure. These are presented in the class (d) number.

In general, the above analyses indicate that there is no significant reliability problem associated with the use of disagreement detectors.

5. STATISTICAL CONFIDENCE INTERVALS FOR MONTE CARLO PROGRAM RESULTS

As previously described, the Monte Carlo prediction program uses a random process to determine a point estimate of a random variable defined as:

$$\overline{R}_{TMR} = \frac{\text{number of successful trials}}{\text{total number of trials}}$$

It is recognized that $\overline{R}_{TMR}$ is a statistical estimate of R_{TMR}, the true but unknown probability of success. The question is to determine how good an estimate.

$\overline{R}_{TMR}$ is random variable (i. e., a number whose value depends on the outcome of an experiment) with mean value R_{TMR} and variance

$$\frac{R_{TMR}\,(1 - R_{TMR})}{N}$$

where N is the number of Monte Carlo games played. If N is large enough to satisfy the inequality

$$N - N R_{TMR} \geq 3 \sqrt{N R_{TMR} (1 - R_{TMR})} \qquad (1)$$

then $\overline{R}_{TMR}$ can be assumed to have approximately a normal, or Gaussian, distribution about its mean, R_{TMR}. A standard normal random variable is created from $\overline{R}_{TMR}$ by the transformation

$$\frac{\overline{R}_{TMR} - R_{TMR}}{\sqrt{\frac{R_{TMR}(1-R_{TMR})}{N}}}$$

Given a confidence level γ, one enters a table of "areas under the standard normal distribution" and finds K_γ, which is the number of standard deviations both sides of the mean needed to include γ of the area under the curve. Then, the probability is γ that

$$-K_\gamma \leq \frac{\overline{R}_{TMR} - R_{TMR}}{\sqrt{\frac{R_{TMR}(1 - R_{TMR})}{N}}} \leq K_\gamma$$

Solving this equation for R_{TMR} gives:

$$\frac{N}{N+(K_\gamma)^2}\left[\bar{R}_{TMR}+\frac{K_\gamma^2}{2N}-K_\gamma\sqrt{\frac{\bar{R}_{TMR}(1-\bar{R}_{TMR})}{N}+\left(\frac{K}{2N}\right)^2}\right]\leq R_{TMR}\leq$$

$$\frac{N}{N+(K_\gamma)^2}\left[\bar{R}_{TMR}+\frac{K_\gamma^2}{2N}+K_\gamma\sqrt{\frac{\bar{R}_{TMR}(1-\bar{R}_{TMR})}{N}+\left(\frac{K}{2N}\right)^2}\right] \qquad (2)$$

To determine the confidence interval for an N-game Monte Carlo simulation, N, $\bar{R}_{TMR}$, and K_γ are inserted into Equation (2). The upper limit for R_{TMR} from Equation (2) is inserted into Equation (1). If the inequality is satisfied, R_{TMR} has a probability of γ of being in the interval given by Equation (2). A typical simulation yielded $\bar{R}_{TMR} = 0.9986$ with N = 10,000 games. With a confidence level or probability of 0.9 (γ), solution of Equation (2) yields

$$0.9979 \leq R_{TMR} \leq 0.9991$$

Inserting of 0.9991 into Equation (1) satisfies the inequality

$$9 \leq 3\sqrt{0.9991 \times 9}$$

Therefore, the probability that $0.9979 \leq R_{TMR} \leq 0.9991$ is 0.9.

G. COMPONENT APPLICATION REVIEW

Component reliability specialists review design and performance specifications as they are published and released by the design areas. This review is used to cross-check the part stress levels against the manufacturer's (or others) data and to ensure that all parts have been appraised by reliability engineering.

Prior to the release of any component part for use in the simplex breadboard, a preliminary review is accomplished through the Component Part Appraisal Request (CPAR). To date, 63 CPAR's,representing 28 component family types, have been reviewed by component reliability.

H. RELIABILITY EVALUATION TESTING

1. MIB EVALUATION TESTING

Twenty-two MIB boards were received in July 1963 for exploratory evaluation; exploratory testing began on 1 August 1963. Three preliminary

measurements were completed: Continuity, Insulation Resistance, and Dielectric Strength. All boards passed continuity tests. During the insulation resistance test, approximately 20 percent of the readings were below the required 1000 megohms. Four out of ten test boards failed dielectric strength tests.

Analysis revealed the dielectric breakdown was caused by voids, poor-quality materials or processes, irregularity of the plated hole walls, and a combination of poor workmanship and quality controls.

Corrective action for each of the problems is as follows:

- Voids in the insulation should be eliminated by a new process procedure.
- Proper holes have been and are being drilled on similar type contracts. Stringent controls are presently being exercised, and process is being monitored during the drilling operation.
- The air bubble-type void in the copper-clad epoxy glass laminate was detected by a dielectric strength test after fabrication of the boards. A dielectric strength test between the two copper sides will be performed during receiving inspection to detect such voids.

Additional MIB boards have been placed on order for re-evaluation.

2. COMMERCIAL MODULES

Exploratory evaluation of 11 commercial modules in the following environments is continuing:

- Humidity
- High and low storage temperature
- Temperature shock
- Vacuum (10^{-6} mm of Hg)
- Power switching

This module type consists of three resistors, four diodes, and one transistor.

Humidity, high and low storage temperature, and temperature shock tests have been completed. There was no significant degradation due to temperature shock. Under moisture resistance test, a general increase in leakage current was noted, and one diode exhibited a 30 percent decrease in breakdown voltage. Changes in all other semiconductors were negligible. Maximum resistor degradation was less than 1.5 percent. No device exceeded end-of-life module requirements.

Vacuum and power switching tests are continuing on schedule.

3. INTEGRATED CIRCUITS (Texas Instruments "Flat-Pack")

Samples of the "flat-pack" were evaluated in a helium environment and subjected to a "zyglo" test to determine the mechanical integrity of the package. Results were inconclusive because of the insignificant amount of leakage. Basically, the package is sound, but there is the possibility of cracking the glass seal around the leads during handling. Additional samples will be evaluated to determine whether special handling procedures are necessary to maintain a "good" seal.

4. URD - TEMPERATURE MATRIX TEST

This test has continued for 2016 hours. Results after 1680 hours are as follows:

Paste Type Overcoat		125°C Max. Drift % at 1680 Hours			
DuPont 7800 paste 500 ohms per square	Sylcyd	3.1	3.1	3.0	2.8
	Glass	6.5	6.2	3.9	4.4
	Diallyl Pthalate	2.5	4.5	3.8	-9
	Epoxy	4.0	4.0	2.0	5.6
DuPont 8000 paste 500 ohms per square	Sylcyd	1.0	1.0	1.0	1.0
	Glass	1.8	2.4	2.5	11.8
	Diallyl Pthalate	5.2	2.0	3.1	3.5
	Epoxy	1.9	1.9	3.1	3.2
Each sample contains 4 resistors, R_1 through R_4.					

All drifts are positive; most samples started with a very high rate of drift which then gradually decreased. This is true except for glass over 7800 paste; the drift rate for these resistors remains high.

As a preliminary indication of long-term drift, some of the resistor values have been projected to 10,000 hours at the apparent drift rate of the last two test intervals (a total period of 28 days). These rates were chosen since, as mentioned, all drift rates appear to be stabilized. Results of this computation are:

10,000-hour predicted drift at 125°C = 1680-hour drift plus observed drift rate × 8400 hours:

Sylcyd	7800:	2.7 to 3.7 percent
Glass	7800:	13 percent
Sylcyd	8000:	0.5 to 1.5 percent
Glass	8000:	5.1 percent

To this must be added the resistance change due to temperature coefficient of resistance for the anticipated operating temperature, which would vary from 0 to 4 percent. The drift rates, while initially positive, have decreased, and the last two readings indicate that they may be becoming negative.

The behavior of the resistors to date suggests the possibility of using a "temperature soak" after trimming to remove the effect of the initial positive drift. The resistors would, of course, have to be trimmed slightly low to compensate for this drift and bring the resistors within initial tolerance. However, if the rate of change becomes more negative such a procedure would be less desirable.

Stability of test and measuring equipment in this test is confirmed by the stability of the Sylcyd-over-8000-paste samples. One additional phenomenon has been brought to light by an unscheduled interruption of power. Some resistors exhibited a change in resistance when subjected to temperature cycling. This suggests the need for a test to evaluate effects of temperature cycling and/or temperature shock.

These tests use temperature only as a stress; the effects of power on drift rate await the results of power tests now being initiated. A much more thorough analysis of test data and TCR will be performed in the next work period.

5. MEMORY EVALUATION

A temperature evaluation test (0-70°C) was conducted on 100 IBM T-38 toroidal memory cores. This test has been instrumental in establishing memory circuit design goals (address and inhibit drivers, sense amplifiers) and dynamic circuit characteristics. A complete report on this test is being prepared.

The electrical effects of mechanical deformation and stress on T-38 core switching performance were investigated. The results of this series of tests are being used in selecting an adequate memory plane encapsulation system and in analyzing the stresses that occur during array operation.

Room temperature evaluation and acceptance testing of 14 unencapsulated 64 × 128 modified-frame planes has been performed to determine marginal or faulty locations.

Temperature and vibration testing has been completed on 10 experimental planes to evaluate encapsulation materials. A 14-plane breadboard array has been temperature-tested while electrically energized.

Progress on these and other component evaluations are reported in the Saturn V computer monthly progress reports.

6. COMPONENT EVALUATION

Effort during this period primarily consisted of consultation service to the design areas in the selection and application of parts. Device capabilities and limitations were provided, and liaison was maintained with vendors to ensure part availability. Information was provided to Quality, Reliability, and Test Equipment Engineering so adequate part inspection and handling procedures could be established.

Major areas of activity were as follows:

(a) Semiconductor chips -- IBM Components Division semiconductor chips will be used exclusively. Requirements for a dual diode and five transistors have been negotiated with the Components Division and the specifications were formally released.

(b) Discrete transistors -- Any discrete transistors to be used in the computer will be of Texas Instruments' "flat-pack" construction. Preliminary investigation revealed that the mechanical integrity of the package is sound, but some concern has arisen as to whether special handling procedures are necessary during equipment fabrication to maintain a "good" seal at the leads. Parts have been ordered for evaluation; the evaluation will be completed in November.

(c) Substrates — The effects of surface finish on pattern adhesion and resistor stability were determined. Investigation revealed that a surface finish in the range of 15 to 60 microinches has no significant effect. Screened resistors and patterns showed no degradation after temperature shock, thermal soak, and rated load testing.

(d) Capacitors — Corning Glass CYFR capacitors will be used for application involving close tolerances and stability. A "stripped" style ceramic capacitor has been recommended for those applications involving moderate stability and tolerances. For decoupling, the Sprague ceramic monolithic, in conjunction with a tantalum type, was recommended.

(e) Page-to-Base Connector — Due to the critical application of this connector, parallel development programs were instituted with Cannon and the Burndy Company. Acceptable proposals were received and negotiated with each vendor. Samples were received and are being evaluated. No insurmountable problems are foreseen.

(f) Cores — Characterization testing of the IBM T-38 core under temperature and vibration was conducted with satisfactory results. Testing was also conducted on cores encapsulated with various materials. Best results were obtained from the Sylgard 183 and Conap 1132 polyester.

Requirements for 95 percent of the component parts have been defined, negotiated with the sources of supply, and drawings prepared. Definition of the remaining parts is dependent on part characterization testing and application review, which are under way and will be completed early in the next reporting period.

Section V

Quality Assurance

Section V

Quality Assurance

A. QUALITY ASSURANCE DRAWING AND SPECIFICATION REVIEW

A procedure for quality assurance review of engineering drawings and specifications was prepared. This procedure will assure thorough and uniform coverage during the engineering documentation review phase of the quality program.

Engineering drawings, specifications, orders,and changes prepared during this period were reviewed for items to be used in the Saturn V program. Some types of items included in the review were: conductor and resistor pastes; substrates; microminiature transistors and diodes (chips); connectors; tape cables; plates; brackets; miscellaneous hardware, resistors; capacitors; cores; plane frames; plane assemblies; ULD's; MIB's; and pages. This review was performed to assure that these documents contain adequate requirements for determining and controlling the quality of parts purchased or produced for this program. Comments, corrections, and recommendations for improvement were forwarded to the respective responsible engineering departments for action. Results of reviews are also being used for inspection and test planning and the generation of inspection and test procedures.

B. CONTROL OF CONTRACTOR-PROCURED MATERIAL

1. SELECTION OF PROCUREMENT SOURCES

A quality assurance program for the control and selection of procurement sources has been initiated. This program has resulted in many meetings to discuss procurement requirements, as well as several liaison trips being made to vendors for close coordination purposes. Liaison trips were made to ensure the quality of items such as the microminiature semiconductor devices (chips), connectors, tape cables, substrates, etc. The records necessary for establishing and maintaining a quality history for each supplier are being continually prepared and maintained. Samples of various items designated for use in the Saturn V program have been obtained from alternate sources and are being evaluated by quality, reliability, and development engineering. In addition, potential vendors are being surveyed to determine their capability for producing a quality product in accordance with all requirements.

2. PROCUREMENT DOCUMENTATION

All purchase orders and procurement specifications are being reviewed by quality engineering to determine that the applicable quality assurance requirements are included and fully defined.

The procurement specification and engineering drawing for toroid ferrite cores (T-38) were reviewed. Corrections, changes, and improvements were suggested and are currently being incorporated. The purchase order for T-38 cores was also reviewed. Pertinent quality assurance requirements were added to this document.

Several meetings and initial negotiations were held with the supplier of chips. Quality assurance philosophies concerning electrical testing, high-temperature storage, lot definition and packaging, visual criteria, bond strength, solderability, and life testing were discussed and defined. Further evaluations must be made of high-temperature storage and life testing requirements. Detail requirements will be developed and included in a procurement specification.

Assistance was given in the formulation of quality assurance requirements for conductor, resistor and substrate materials. These requirements have been included in engineering specifications and material control acceptance procedures.

3. RECEIVING INSPECTION

a. Procedures

The generation of receiving inspection procedures (detail inspection procedures and general inspection procedures) is continuing. A major effort in this area has been directed toward the generation of procedures for the receiving inspection of microminiature semiconductor chips, substrates, resistor pastes, and conductor pastes. Procedures for the receiving inspection of other raw materials are also being generated.

Detail inspection procedures are being written on parts and components as the applicable drawing and purchase orders are reviewed by quality engineering.

b. Equipment

The methods and equipment required for the receiving inspection of substrates have been investigated. The necessary additional equipment required (comparator charts and holding fixtures) were designed and made available in June 1963. A finalized inspection procedure was also released at this time. A roto-viscometer has been purchased for use in the receiving inspection of resistor and conductor pastes. The viscosity of these materials has been found to be a critical factor in the screening of substrates to fabricate ULD's.

Analysis is being continued on the development of other required receiving inspection methods and equipment. As these methods and equipment are developed, they will be made available to receiving inspection for use.

c. Drawings and Specifications

A continuing effort is being exerted in this area to ensure that all drawings and specifications are adequate, to the proper level, and available for receiving inspection purposes.

d. Chemical Analysis and Physical Tests of Purchased Items and Raw Materials

All raw materials purchased for the Saturn V computer are subjected to a chemical analysis upon receipt in accordance with the applicable engineering specifications and material control acceptance procedures.

Physical testing is being performed on items received as required by the applicable general or detail inspection procedure.

e. Failure and Deficiency Feedback

Inspection was begun on initial receipts of substrates, conductor and resistor pastes, connectors, plates, discrete electrical components, copper clad epoxy sheets, encapsulating materials, solders, and fluxes, for use in the first breadboard computer. Items are being inspected as they are received. Any defects are immediately reported to the supplier via the "Rejected Purchase Report." This report relates the items received from the vendor, items inspected, items rejected, a breakdown of the defects by number and type, and a request for immediate corrective action. In addition, under the Supplier Rating System, each supplier receives a "Monthly Conformance Report" which indicates his conformance rating in regard to quality and delivery. This points out the deficiencies that exist in the quality of his product. Suppliers whose products consistently fail to meet quality standards are recommended for suspension from the suppliers' list.

f. Records

Adequate records of all receiving inspection results are continually being prepared, analyzed, and maintained.

C. CONTROL OF CONTRACTOR-BUILT ARTICLES

1. INSPECTION AND TEST PLANNING

The URD, ULD, MIB, page, memory plane, memory array, and memory unit manufacturing processes were defined emphasizing the quality aspects. The proposed inspection and test points for the above items were selected. The fabrication levels at which major quality criteria for product "acceptance" will apply have been established (e.g., ULD, MIB, page, etc.). The necessary in-process and final inspections and tests were incorporated in the manufacturing process procedures and manufacturing orders (routings) to aid in controlling the process. Process flow charts of control plans for the ULD and MIB process were prepared to detail the fabrication and inspection operations and the type of inspection and test operations to be performed. After each of the major fabrication operations, a complete inspection will be performed. As more confidence in the process is assured through improved controls, sampling inspection of certain operations may be instituted.

Investigations and studies were conducted jointly by quality and reliability personnel to formulate in-process and final testing plans for chips, URD's, MIB's, pages, memory cores, planes, arrays, and memory units. Testing philosophies have been established and agreed upon, with the exception of burn-in of semiconductors. This requirement is being further evaluated. Many of the detailed testing requirements were evaluated. Some remain to be evaluated in the next period.

2. CONFORMANCE CRITERIA

Inspection and test procedures, defining the: (1) characteristics; (2) accept-reject criteria; (3) tests; (4) test conditions; (5) measurement method; (6) frequency; (7) equipment; (8) degree; and (9) duration and number of tests, were prepared for the various levels of ULD, MIB, and memory plane inspections. Where applicable, the written criteria is supplemented by visual aids representing acceptable and unacceptable workmanship, and made available for use by line manufacturing and inspection personnel.

3. INSPECTION AND TEST PERFORMANCE

In-process inspection, quality surveillance, and investigations on the ULD, MIB and memory plane manufacturing lines are continuing to collect

the information and experience necessary for quality assurance to control the various processes. Quality control resistor drift analysis sheets and a plan were designed and are being used in ULD fabrication. These sheets are designed to detect drifts and the magnitude of drifts in resistor electrical parameters that have been created by the production process at various selected levels. Failure analysis reports on ULD's are being reviewed to determine the failure mode and mechanism. These reviews are matched against inspection procedures to assure that inspection criteria, methods, and techniques are adequate. Initially, these inspections and analyses revealed a high reject and fallout rate. Intensive investigations by quality engineering resulted in recommendations for modifications and changes in tooling, process procedures, Engineering documentation, and inspection procedures. Also, operators have received additional instructions on several operations so that they may perform more effectively. Consequently the defect rate has been reduced considerably on many operations. Evaluation is continuing to reduce this rate even more drastically.

4. PROCESS CONTROLS

In addition to the process flow charts previously discussed, manufacturing orders (routings) and manufacturing process procedures are utilized as aids in controlling the manufacturing process. Routings assure callout of proper sequence of manufacturing and inspection operations, departments responsible for operations, proper processing procedures, tooling, materials, conditions of manufacture and engineering change level.

Routings and process procedures are reviewed by quality assurance as they are prepared for completeness and adequacy prior to their implementation in the manufacturing line. Quality assurance procedures are generated and implemented, as required, to supplement other controls over various processes; such as, soldering and tinning, encapsulation, plating and solution control. A URD resistor experiment is being performed to determine the effectiveness of the following: (1) present process controls; (2) resistor parameter drift during the manufacturing process; and (3) the effects of resistor and conductor paste viscosities. The various processes were monitored by quality assurance during this period.

5. QUALIFICATION OF PROCESS OPERATIONS

A quality assurance procedure for the qualification of the ULD and MIB process system (which includes operators, inspectors, tools and procedures at each operation) was prepared. This procedure, to be implemented during the next period, will ensure that a quality product is produced. It is planned to extend the use of this procedure to other processes.

D. INSPECTION, MEASURING, AND TEST EQUIPMENT

1. STANDARD TEST EQUIPMENT

This equipment is periodically checked and calibrated in accordance with the standard plant operating procedure. This equipment is initially checked upon receipt for accuracy and adequacy for performing the required inspection operations.

2. SPECIAL TEST EQUIPMENT

a. Calibration

Two ULD testers are now on location in the test area. One ULD tester has been fully checked out and is presently being used to evaluate test tapes. The second tester has been partially checked out.

b. Evaluation

A preliminary inspection and test philosophy has been established for test equipment (LTE and FTE). The plan provides visual, mechanical, and electrical criteria at all the proposed levels of inspection. These include receiving inspection, process inspection, evaluation, calibration-certification, acceptance, and shipping. Detailed criteria are being developed for each of these areas.

Quality assurance assistance was provided in evaluating and programming the first Saturn V ULD tester. Test specifications were reviewed and inputs were provided on manufacturing improvements which should be implemented to improve tester operations. The review of the design and performance specification for the ULD test set has been completed. Twenty-six ULD test tapes have been functionally checked and the errors have been corrected. Errors were reported to test equipment engineering for corrective action.

The design review of the special circuits tester has been completed.

The design audit on the Circuit Page Tester was initiated and is continuing.

The design audit of the ACME test equipment has begun.

c. Written Procedures

All released test specifications are continually being reviewed and errors are being corrected.

All URD test operations have been reviewed and evaluated.

The review of the ULD test specifications is continuing as these specifications are released.

The resistor trimmer test procedure was received, reviewed, and evaluated.

d. Records

Records are being maintained which indicate the date of the last calibration and the due date of next required calibration for all test, inspection, and measuring equipment.

The results of inspections and evaluations of all inspection, measuring, and test equipment are being documented for the purposes of analysis and review.

E. HANDLING AND STORAGE

Quality assurance monitoring of inspection results and defect rates has indicated many rejects due to inadequate handling techniques and storage facilities for this technology. The problem areas were studied, and improved handling techniques were developed. New handling and storage facilities have been and are being procured to eliminate the problem areas.

All procurement specifications, to be released, are being reviewed to determine if adequate handling and storage provisions have been included. Handling and storage operations will continue to be analyzed to ensure that they will result in no detrimental effect on the quality of the product.

F. TRAINING AND CERTIFICATION OF PERSONNEL

A thorough investigation of the requirements for a personnel training and certification program was conducted. A general procedure has been prepared for the program, which includes requirements such as: responsibilities; training; testing; identification; certification; maintenance of status; recertification; and auditing. A detailed investigation was made to determine which fabrication and inspection operations are of a specialized nature, having a significant effect upon the quality of follow-on computers, and would require certification. The operations requiring training and certification consist of the major fabrication and inspection operations.

G. DATA REPORTING AND CORRECTIVE ACTION

1. QUALITY DATA

Records are maintained of inspections and tests performed throughout the entire development, receiving inspection, fabrication and assembly process. The records provide evidence that the required inspections and tests have been performed. These tests include: (1) part, component, or assembly identification; (2) inspection or test involved; (3) number of conforming articles; (4) number rejected; (5) nature of defects; and (6) basic causes for rejection. These records cover both conforming and defective articles.

A new name and defect code listing has been generated for characteristics peculiar to ULD production. The new codes are utilized with the present quality control data retrieval system and will provide a standardized method of reporting factual and timely information on actual and potential problem areas.

Weekly quality control summary reports were generated. These reports indicate total inspected, total accepted, total rejected, percent defective, defects by operation and type, major problems, causes and corrective action.

2. CORRECTIVE ACTION

As deficiencies or failures are detected, they are investigated and analyzed to determine the cause. Responsible design, reliability, quality control, manufacturing, or supplier organizations are immediately notified that corrective and preventive action is required. This action is taken and documented. Any rework operations are documented and closely controlled. A subsequent review is made to determine the adequacy of corrective action taken, and each deficiency is noted in reports until the corrective action has adequately resolved the problem.

H. INSPECTION TECHNIQUES

A study was made to determine the applicability of using either a proficorder or a light section microscope to measure screened conductor and resistor thickness. As a result, a proficorder was chosen for this inspection operation. A study was made to determine the applicability of the optical comparator with the high-intensity light reflectance attachment to Saturn V inspection technology. This item of equipment was found to be extremely desirable for use in the visual inspection of ULD's and MIB's at various levels. A study was also made to determine a fast, accurate and effective method of inspecting the Laminar X-500 coating sprayed on screened ULD resistors. ultraviolet light, with microscope spot adapter, was chosen for this inspection operation.

Section VI

Maintainability

Section VI

Maintainability

Accomplishments from April through September 1963 are as follows:

(1) Observed the facilities layout and operational capabilities of the NASA laboratories. Discuss the LTE requirements, testing requirements for NASA laboratories, prototype computer and data adapter, and associated topics with IBM Huntsville and NASA personnel.

(2) Generated a reference designation standard for the computer. This standard provides a simplified method for establishing component reference designation of this unit.

(3) Originated and submitted to the LTE design area, a design for a ULD page test-point adapter for inclusion as a tool required with the LTE. This tool will enable the LTE operator to gain access to the ULD page test points without removing the page from the unit.

(4) Conducted a study to determine the need for handling devices, necessary for general handling activity, and to aid in installing the data adapter and computer into the IU compartment of the Saturn V vehicle. A preliminary handling device requirement at various locations (depot, MSFC, and MILA) was originated and submitted to various IBM design groups and discussed with NASA personnel at IBM. The data adapter, computer and LTE design efforts are being coordinated to ensure the compatibility of these handling device designs. Further coordination with NASA personnel is contemplated for compatibility of IU installation of the computer and data adapter.

(5) Originated and released the maintainability requirements specification for the computer and data adapter to IBM Space Guidance Center, Huntsville, and NASA/MSFC personnel. These specifications establish the maintainability design requirements, compatible with the over-all maintenance concept, and define other associated maintainability program features.

(6) Continued to assist the computer, data adapter, and LTE design groups to ensure the incorporation of maintainability features which are consistent with the maintainability requirements established in the maintainability requirements specifications.

Those activities which are still in process are as follows:

(1) A study of the launch-pad check-out requirements for the Advanced Guidance and Control System is in process. The results of this study will be discussed with IBM Engineering and NASA personnel to formalize the launch-pad check-out requirements and to establish the necessary procedures to fulfill these requirements.

(2) The Saturn V maintenance plan, which presents a consolidated program for the computer, data adapter and LTE, has been revised and updated to conform to the design changes and will be continually updated as the program progresses.

Section VII

Factory Tools and Test Equipment

Section VII

Factory Tools and Test Equipment

A. GENERAL

The over-all Saturn V manufacturing engineering program is proceeding on schedule. In summary, the most significant accomplishments during this reporting period were:

- Tooling up and establishing a ULD fabrication line.
- Establishing an integrated photographic tool generation facility for MIB's.
- Setting up the IBM Components Division as a source for all prototype and production ULD's.

1. SPECIAL CIRCUITS TESTER DEVELOPMENT

A quantity of special pages, memory panels, and miscellaneous circuit assemblies which require special considerations in the testing operation, need a special program board-environmental chamber combination. The environmental chamber is an oven containing interchangeable fixtures to allow the various assembly configurations to be tested. The special testing considerations of short lead lengths, fast rise times, etc., necessitated a special fixture and program panel with a rack of commercially available equipment. All equipment was consolized to facilitate this testing operation. This test set will be used in the engineering laboratory to test page assemblies for the breadboard computer.

2. RESISTOR TRIMMING SIMPLIFIED PROGRAM SYSTEM

IBM found it necessary to develop a programming system to be used with the Manual Resistor Trimmer to simplify the writing of input data. The trimmer program consists of the following: (1) the Coding Form, (2) the Compiler Program, and (3) the Paper Tape Producing Program. A 1401 Data Processing System is needed to process these tapes.

The Coding Form was designed to facilitate writing the Compiler Program input data. The objectives of the Compiler Program are (1) to eliminate manual calculations necessary to produce the input data for the trimmer, and (2) to supply the engineer a printed report of the test being made. The Paper Tape Producing Program reads the magnetic tape output produced by the Compiler Program into the IBM 1401 Core Storage. This program converts the data into the proper format for an input to the trimmer and then directs the IBM 1012 Tape Punch to produce a paper tape. This paper tape is the primary output of the Resistor Trimmer Programming System and is used as an input to the trimmer.

3. PALLET

The development of the fixture needed to test ULD's on the Semi-Automatic Circuit Test Set created a need for a holding device for the ULD while under test and for ease of handling. The pallet is made of fibrite material and can withstand the temperatures required for the ULD Environmental Test. The pallet was designed in two pieces, with a top and bottom form identical except for the holding ears. This pallet can also be utilized while the resistors on the substrate are being trimmed. IBM plans to use this device during the follow-on prototype program.

4. MANUFACTURING ENGINEERING

Manufacturing engineering has established liaison and print review of all component and assembly drawings, prior to their release from development engineering, to ensure good manufacturability and design at minimum cost.

This includes pre-analysis of the designs for proper materials, dimensional conformity of detail hardware to assure good subassembly and assembly aspects, and proper specification application.

Where necessary, routings have been established on all fabrication levels to assure proper engineering control during the complete manufacturing cycle.

Hard tools for machining, assembly, and inspection purposes have been designed, fabricated, and incorporated in all areas as dictated by the manufacturing engineering analysis of released parts. To minimize possible damage to miniature components (mechanical and electrical), special handling devices and storage units were developed and placed into use.

Capital equipment justifications, facility flow analysis and preliminary layouts were developed.

B. SIMPLEX ULD's

1. MODIFICATION OF TWO GEMINI SEMI-AUTOMATIC CIRCUIT TEST SETS (SACTS) FOR ULD TESTING

Two Gemini SACTS were converted and retrofitted from the Gemini Program to allow testing of ULD's at 25°C, 0°C, and 100°C. Fixture contacts were designed and developed for making connection with the module substrate. The Gemini Programmer Comparator 1620 Compiler Program was revised for use on the Saturn V. The generation of program tapes and plugboards required to test 39 ULD types is approximately 50 percent complete. Calibration of both SACTS is complete and the machines are operational. (See Figures 7-1 and 7-2.)

2. MANUAL RESISTOR TRIMMER (Figure 7-3)

The Manual Resistor Trimmer prototype was revised for the Breadboard Program use in the form of electronic changes and a completely new trimming fixture. The trimmer operates from a punched tape input and template guide. A purge system was inserted in the nozzle of this fixture to clean out any buildup of abrasive. The trimming operation and subsequent manufacturing operation was evaluated as to the effects on the final resistor values. Operators trained in the use of this trimmer are now proficient in producing quality parts. The evaluation of the trimming operation is a continuing effort and shall remain so until all module types have been evaluated. Seven of the 39 types have thus far been evaluated.

3. ULD FABRICATION

A single-purpose semiclean area, combining manufacturing, assembly and testing of ULD's has been established and placed into operation. This consisted of providing the work area itself, as well as all the necessary mechanical and electrical tools and equipment required for the ULD fabrication process.

4. ULD MANUFACTURING

ULD manufacturing process procedures have been developed and released for the following: (1) substrate cleaning of edge, top, and bottom; (2) conductor pattern screening; (3) resistor screening; (4) firing of patterns; (5) dip soldering of edge, top, and bottom; (6) leadless chip mounting; and (7) encapsulation.

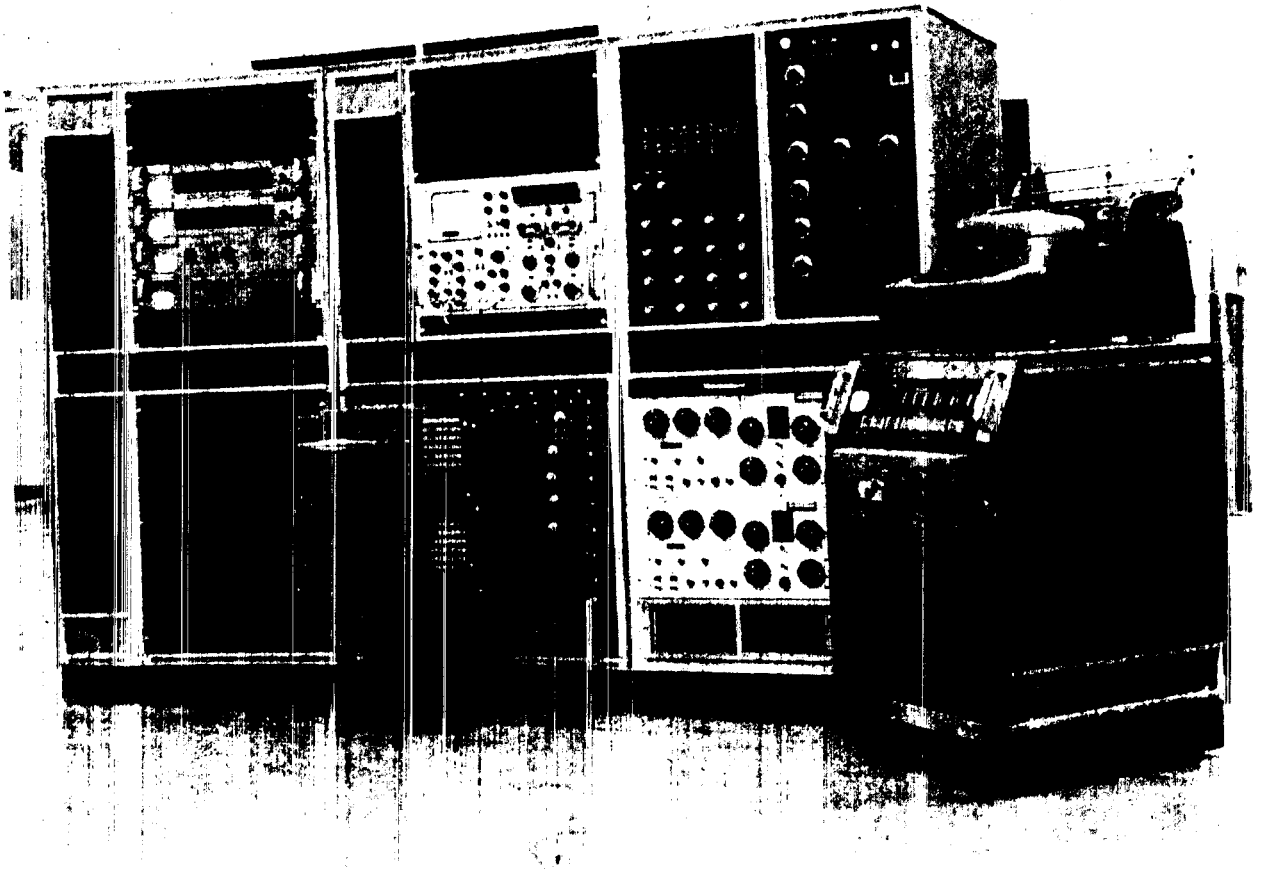


Figure 7-1. Semi-Automatic Circuit Test Set

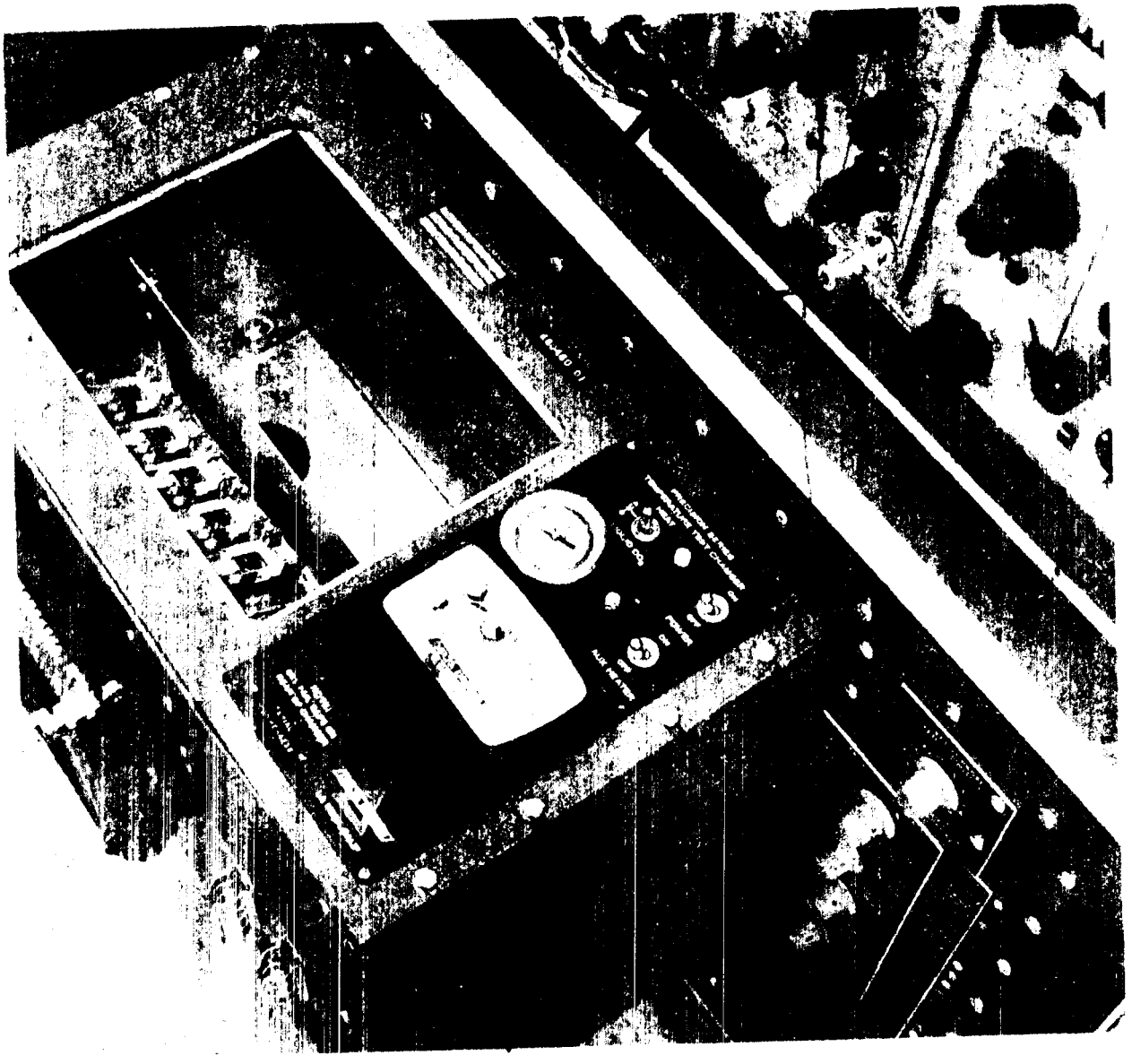


Figure 7-2. Semi-Automatic Circuit Test Set Temperature Test Chamber

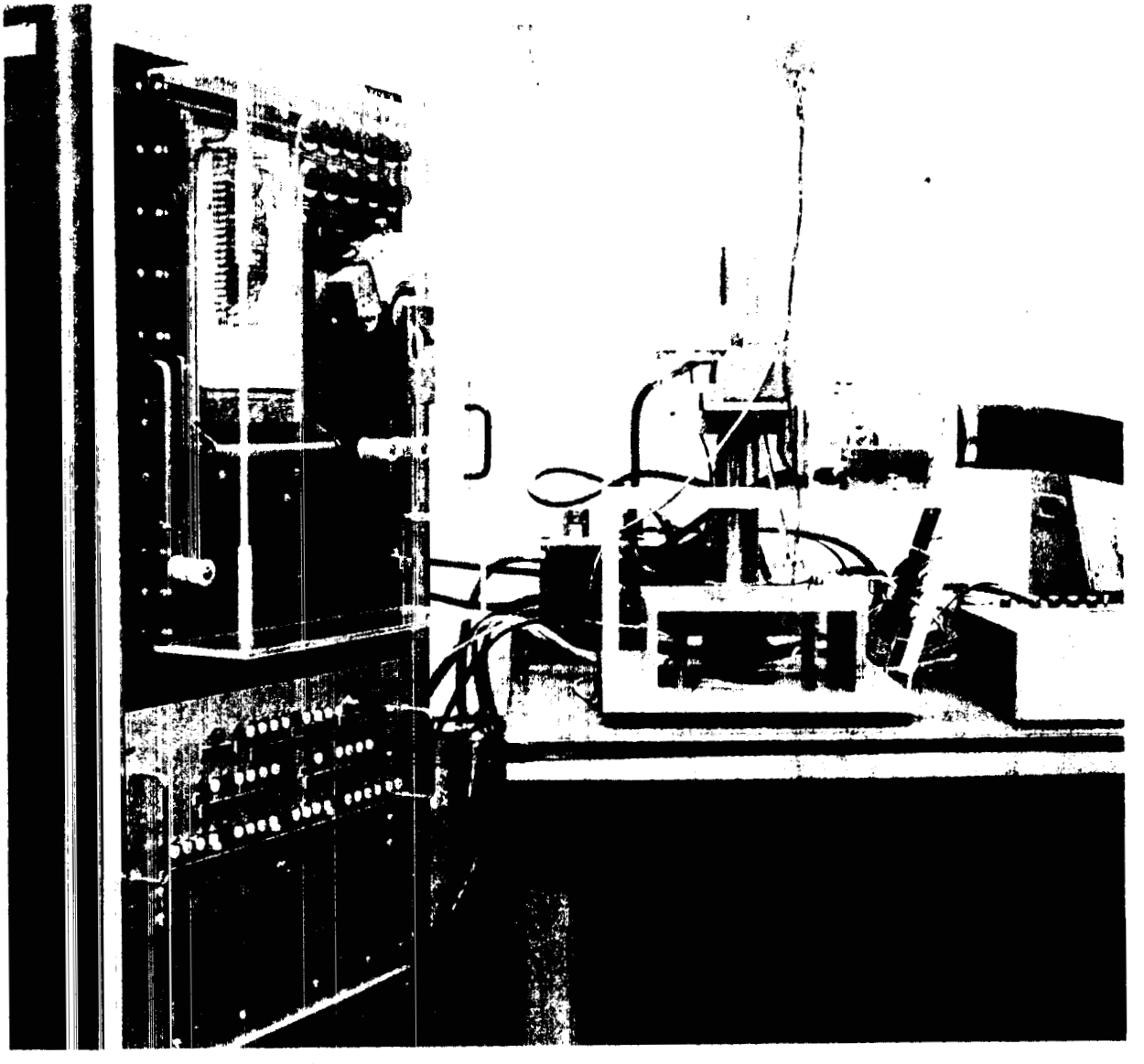


Figure 7-3. Manual Resistor Trimmer

a. Process Procedures

Process procedures are being upgraded as a result of production line experience, new knowledge of processing effects and materials, and changes in engineering specifications. Manufacturing personnel have been trained and are qualified to perform the various tasks required to produce the ULD's for the Saturn V computer.

Development of processes for screening conductor and resistor patterns required extensive analysis and testing of screen wire size and mesh for various viscosities. Separate optimums in screen and paste viscosity were developed for conductors and resistors. Squeege angle, pressure, sharpness, and rate were investigated to determine optimum tool design and process control.

b. Cofiring of Conductors and Resistors

Cofiring of conductors and resistors was thoroughly investigated with the intent of reducing processing variables, number of operations, and costs. Conductor adhesion was insufficient for reliability requirements at the lower temperature necessitated by resistor-paste temperature tolerance.

Processes for screening and firing were released on 5 September 1963. Tighter controls on screening development will result as additional experience and knowledge in production is accumulated. Firing charts and logs have been developed to reduce the time required to determine the firing temperature for various module designs.

The viscosity of screening pastes has been checked daily to reduce excess we porosity and conductor fissures.

Since firing of leadless devices caused the conductor pattern to dissolve into the solder, the processes and tools were revised. Adequate masking tools for this high temperature were extremely difficult to develope. Conventional resistor overcoats degraded at this temperature; therefore, it became necessary to delay the resistor overcoat application until after the dip solder conductor application. A screened glass frit masking operation was developed to augment the tool masking. The solder application process was released on 10 September 1963.

Chip mounting procedures, involving reflowing in the BTU conveyor furnace, were released on 17 September 1963. Funding limitations required the development of a similar process for a static muffle furnace, which offers an offsetting advantage of reduced cover gas consumption.

c. Soldering Techniques

A surface-solder application was developed on the flow solder machine, followed by a dip-solder application to edge and bottom patterns. To take advantage of the added reliability of leadless devices in place of flying lead devices, these processes had to be scrapped in favor of dip soldering due to the excess temperatures required in flow soldering 10/90 solder.

d. Encapsulants

Considerable effort has gone into investigation of various encapsulants and mold tool designs which will not cause excessive exotherm, voids, vacuum evaporation, chip device destruction, and which have reasonable thermal expansion matching and bonding characteristics to the ceramic substrate. An RTV-60 process procedure was released on 2 August 1963. Further development is being carried out to reduce fallout resulting from this operation.

e. Marking Equipment

Marking equipment has been procured and tested. The fixtures will be modified for finalization of this process.

C. MEMORY

The single-aperture toroids have required effort in assisting with both temporary and in-house mold design, as well as with matrix plate and covers to accommodate the existing OAO-Gemini frame. Support in drilling experiments for the frame ear holes was provided. Curing fixtures were tested and modifications recommended for additional tooling.

D. MIB's

The MIB manufacturing engineering project has been established to support the fabrication of MIB's for the following:

- Process requirements
- Glass tools (from artwork)
- Process tools
- Process development
- Tool engineering and design support

Facilities have been provided to generate artwork and provide photo processing. Layer and MIB fabrication employ a photo-resist technique. This method reduces the cost of tooling required when compared to silk screening, as well as reducing the manufacturing cycle. A new exposure-printer has been set up and is operational for this process.

The amount of product work accomplished is as follows:

- Artwork and Photographic Processing

  1:1 Film — Detail drawings to Engineering for release

  Completed 26 MIB's — 32 MIB's in process

- Pattern Application

Layers	760 in stock (including 724 for special test, reliability analysis, and test equipment)
MIB's	2 in process

- Production Tools

  Total - 36 tools

Completed	10 — working and functional
On schedule	23 — in design or build
Behind schedule	3

E. STRUCTURE

Manufacturing engineering conducted an investigation to determine the best means of building the liquid-cooled structure as an assist to development engineering. The two methods under consideration are: (1) Machining the housing from a solid billet and gun drilling the cooling lines, and (2) preforming stainless steel tubing to the cooling flow required and casting this as an integral part of the housing.

F. PAGES

To further assist development engineering, manufacturing engineering designed, built and evaluated a page extraction tool for system use. The extractor provides a mechanical means of removing a single page of electronics by containing the page at its extremities and applying equal pressure, thereby eliminating any damage to the connector end of the page.

Due to the lack of parts, effort has been limited on the ULD-to-page attachment. Areas of investigation include infrared and hot reducing gas solder reflow. Experimental tooling is being developed for low-temperature edge solder dip application, following chip device reflow firing. This presents an extremely difficult masking problem.

Experimental tooling is also being developed for solder preforms, as an alternate backup to adding solder by dipping. This technique will be investigated as tooling and preforms become available.

G. ULD PROTOTYPE PROGRAM

1. GENERAL

IBM's program is a complete component program to engineer and manufacture miniature circuit modules for use on the Saturn V prototype and production programs. The present program calls for shipment of 61,000 ULD's. The shipment is scheduled to begin in January 1964 and end in July 1964.

2. CIRCUITS/SPECIFICATIONS

The IBM Components Division has signed off on six different semiconductor chip specifications submitted by the IBM Space Guidance Center for populating ULD modules. The six types are:

IBM P/N	Description
6000043	Medium-Speed, Logic Transistor
6000044	Medium-Speed, High-Breakdown Transistor
6000045	Matched-Pair, Low-Speed Transistors
6000046	Low-Speed, High-Breakdown Transistors
6000047	Medium-Speed, Dual Diodes
6000048	Medium-Speed, High-Breakdown Transistors

The IBM Space Guidance Center has submitted 12 ULD electrical specifications to the Components Division for review and concurrence. Thirty-nine specifications will be submitted by 4 October 1964.

Work has started to obtain and maintain data and curves correlating the $25^{o}C$ in-house limits to the 0 and $100^{o}C$ specification points.

3. DEVELOPMENT

a. Edge Clip Development

Preliminary tools are completed for the fabrication of two types of end around clips:

- An "H" clip — rigid connection to MIB - single thickness elevation of substrate-difficult to trim waste.
- An "S" clip — flexible connection to MIB - double thickness elevation of substrate - easy to trim waste.

Substrates with "H" clips have been pull tested at the IBM Space Guidance Center. The land patterns on these substrates were fired at 760°C. The pulls ranged from 33 to 52 pounds. ULD's with no end arounds, and land patterns fired at 960°C are reported to range from 47 to 49 pounds. The following two facts are important.

- When the "h" clip substrates failed, the land pattern pulled away from the substrate.
- Data from the IBM Space Guidance Center shows that pull strength improves about 1.7 times when lands are fired at 960°C rather than 760°C.

New samples were received for testing at higher firing temperatures. In addition, vibration tests for these samples are being set up. Completed modules are on hand for added reliability testing as required.

This project should be complete by 1 November 1963.

b. Encapsulation

Potential problems in transfer molding over RTV or other silicones are space limitations, thermal shock, and decomposition of the transfer mold material on the 150°C 500-hour burn-in or the vacuum bake at 100°C.

A definite problem with single coats of silicones would be chlorinated solvent resistance, since silicones are inherently weak in this respect. Since the IBM Space Guidance Center specification states that chlorinated resistance is not required, the Components Division specification pertaining to chlorinated resistance should not apply. Single coats of polyurethanes are unlikely to be acceptable for thermal stability or T-H resistance.

The following preliminary tests are scheduled to begin in October:

- Transfer mold over RTV.
- Transfer mold over silicone
- Single coat of silicone
- Hermetic seal (December)
- RTV over slurry
- Polyurethanes

Appendix

Failure Rate Change Justification

Appendix

Failure Rate Change Justification

Some of the failure rates used in the initial Saturn V reliability assessment have since been revised. This appendix describes those changes.

A. MIB's AND BACK PANELS

Estimated average failure rates for MIB's and back panels have been changed to reflect the latest design information. Figure A-1 and Tables A-1 and A-2 show how the current rates were computed.

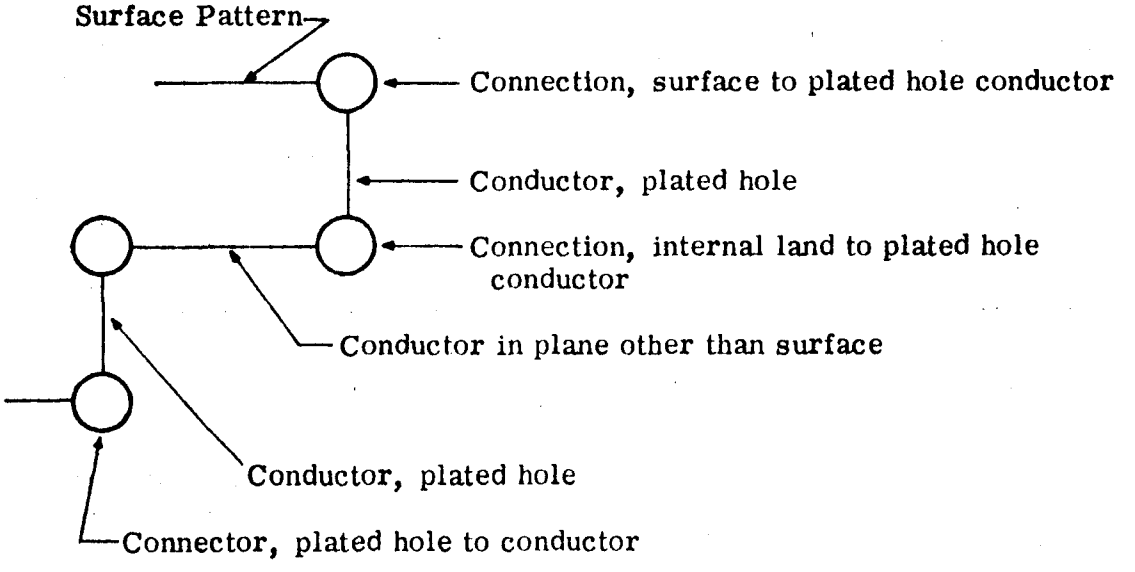


Figure A-1. Typical MIB Connection Configuration

Table A-1

MIB Failure Rate Determination
(28 ULD's/MIB)

	Number	Failure Rate (Failures/10^6 hrs)	K_s*	Total Failure Rate
Surface Pattern (for ULD)	300	0.00001	0.50	0.003
Surface Pattern to Hole Connection	280	0.0006	0	0.168
Conductor Pattern (in hole)	300	0.00001	0	0.003
Hole to Internal Pattern Connection	349	0.001	0	0.349
Conductor Pattern (in conductor layer)	300	0.0001	0.13	0.030
			Total	0.553
*K_s = Conditional probability of short-mode failure				

NOTES:

$$\text{Total } K_s = \frac{0.13 \times 0.03 + 0.5 \times 0.003}{0.553} = \frac{0.0054}{0.553} = 0.0098$$

Probability of short = 0.01
Probability of open = 0.99

Table A-2

Back Panel Failure Rate Determination

	Number	Failure Rate	K_S*	Total
Surface Pattern to Hole Connection	2200	0.0006	0	1.32
Hole to Internal Pattern Connection	2200	0.001	0	2.20
Conductor Pattern (in conductor layer)	2200	0.0001	0.13	0.22
Conductor Pattern (in hole)	2200	0.00001	0	0.022
			Total	3.762

*K_S = Conditional probability of short-mode failure

$$\text{Total } K_S = \frac{0.13 \times 0.22}{3.762} = \frac{0.0286}{3.762} = 0.0076$$

B. MONTE CARLO FAILURE RATE ADJUSTMENTS

The following tables list the hardware utilized in the Saturn V computer, and the end result of the reapportionment technique. A description of the actual technique may be found in the initial reliability assessment report (IBM No. 63-394-062).

Table A-3

Hardware Listing

Item	Number (n)	$\lambda \times 10^6$	K_o	$n\lambda_o \times 10^6$	$n\lambda_s \times 10^6$	$n\lambda \times 10^6$
Back panel	5	3.762	0.8	15.048	3.762	18.810
Flexible cable	120	1.0	0.9	108.0	12.0	120.0
Pages	54	1.106	0.8	47.78	11.95	59.73
Connectors, bodies	64	0.003	1.0	0.192	-----	0.192
Connectors, pins	6272	0.007	0.8	35.12	8.781	43.901
Substrates	2472	0.0245	1.0	60.56	-----	60.56
		Totals		266.70	36.493	303.193

Component lead count, per system = 57,258

$$\Delta\lambda_o \cong \frac{\lambda o}{L} \cong 0.00466 \times 10^{-6}$$ (adjustment factor to be added to probability of open for each component lead)

$$\Delta\lambda_s \cong \frac{\lambda s}{L} \cong 0.00064 \times 10^{-6}$$ (adjustment factor to be added to probability of short between component terminals)

Table A-4

Reapportionment Table

Item	No. of Leads	Factor to be Added to Each Component Failure Rate		Total Adjustment Factor
		$\lambda_O \times 10^6$	$\lambda_S \times 10^6$	$\lambda \times 10^6$
Transistor	3	0.013974	0.001912	0.015886
Resistor	2	0.009315	0.001275	0.010600
Diode	2	0.009315	0.001275	0.010600

Table A-5

Adjusted Failure Rates and Conditional Probability of Open

Item	$\lambda \times 10^6$	K_O
Transistor	0.027886	0.6646
Resistor	0.02359	0.7917
Diode	0.01659	0.7279

Table A-6

Single Channel Timing Generator Failure Rates

Item	No.	$\lambda \times 10^6$	$n\lambda \times 10^6$
Transistor	224	0.012	2.688
Resistor	289	0.019	3.757
Diode	90	0.006	0.54
Pages	2-2/3	1.106	2.9493
Substrates	106	0.0246	2.6076
Conns.	2-2/3	0.689	1.8371
		Total $\times 10^6$ =	14.36946
$\therefore R_{TG} = e^{-14.36946\ T \times 10^{-6}}$			

Table A-7

Single Channel, TMR Logic Substrate Failure Rate

Item	No.	$\lambda \times 10^6$	$n\lambda \times 10^6$
Clip	12	0.0005	0.0060
Ball joint	10	0.0005	0.0050
Solder fillet	12	0.001	0.0120
Single side land	15	0.0001	0.0015
Substrate base	1	0.0001	0.0001
		Total $\lambda \times 10^6$ =	0.0246

Table A-8

Single Channel, Logic Component Count

Item	No.	$\lambda \times 10^6$	$n\lambda \times 10^6$
Page	18	1.106	19.89
Flexible cable	40	1.0	40.0
Connector	22	0.689	15.158
Back panel	1-2/3	3.762	6.283
Substrate	824	0.0246	20.27
Delay line	2	0.3	0.6
Transistor	680	0.012	8.16
Resistor	4240	0.006	25.44
Diode	2503	0.013	32.530
		Total	168.34

$\therefore R_{SL} = e^{-168.34\ T \times 10^{-6}}$